FIG. 1

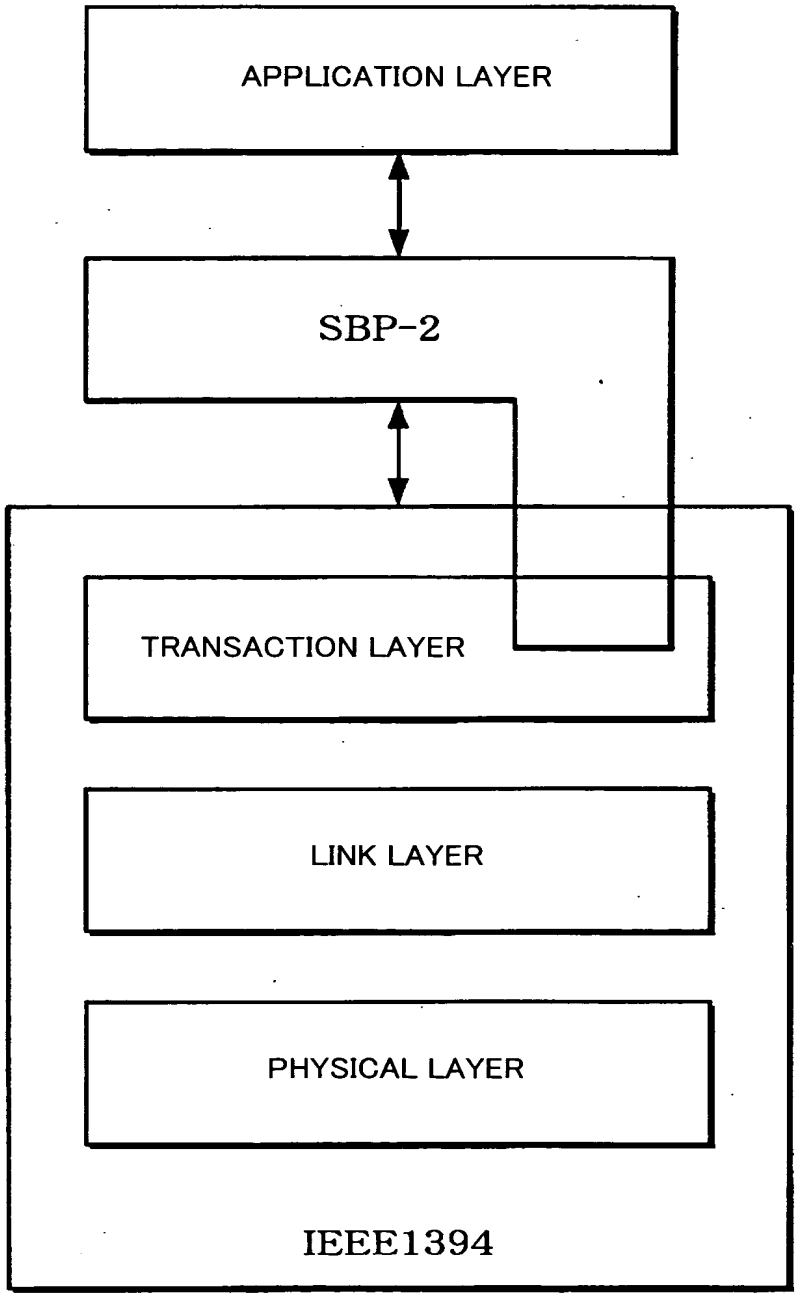

APPLICATION LAYER
SBP-2
TRANSACTION LAYER
LINK LAYER
PHYSICAL LAYER
IEEE1394

FIG. 2

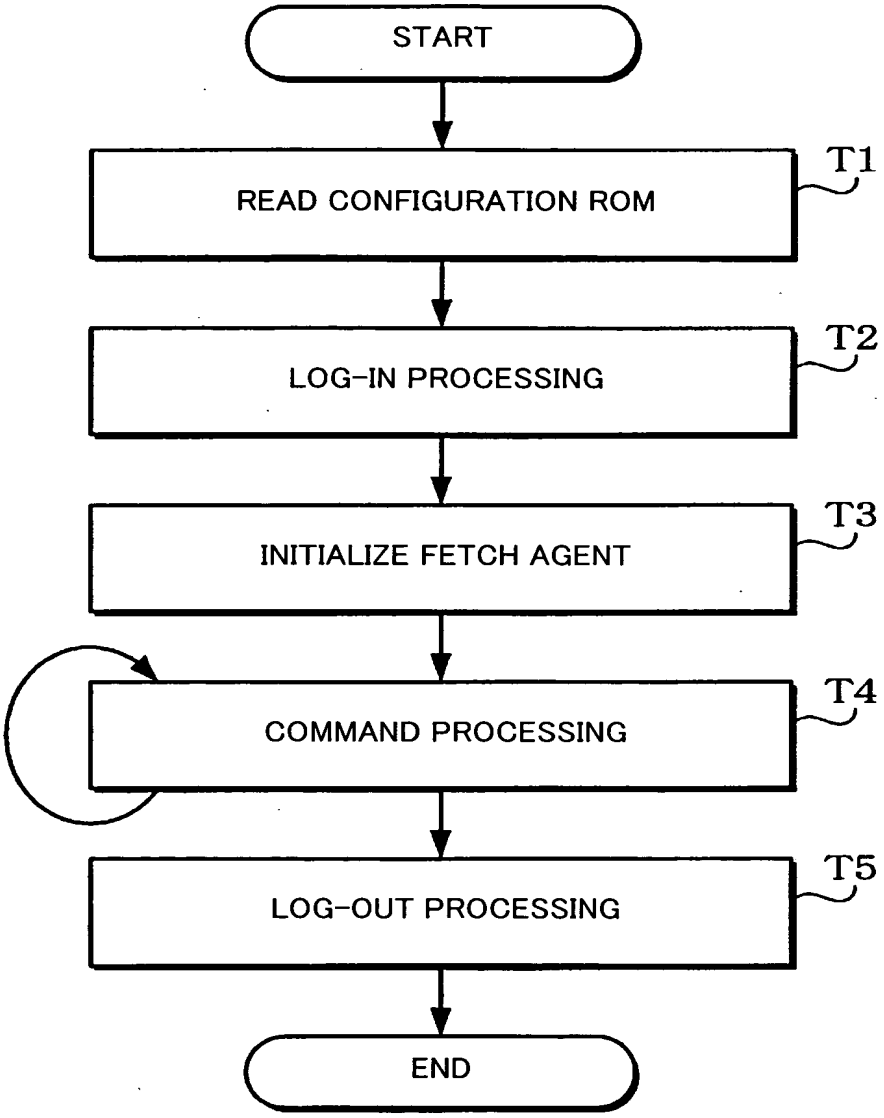

START
READ CONFIGURATION ROM
T1
LOG-IN PROCESSING
T2
INITIALIZE FETCH AGENT
T3
COMMAND PROCESSING
T4
LOG-OUT PROCESSING
T5
END

FIG. 3

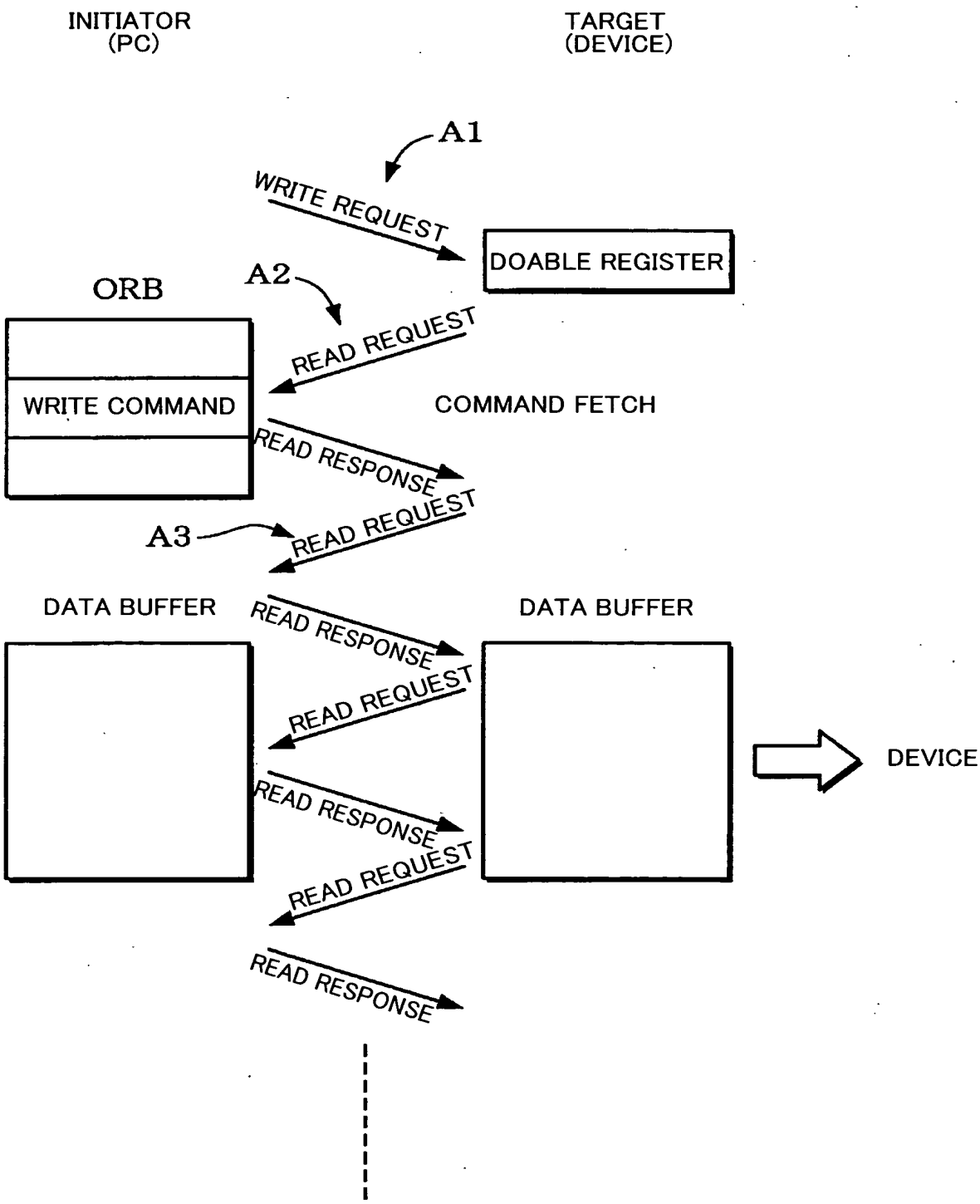

INITIATOR
(PC)
TARGET
(DEVICE)
A1
WRITE REQUEST
DOABLE REGISTER
ORB
A2
READ REQUEST
WRITE COMMAND
COMMAND FETCH
READ RESPONSE
A3
READ REQUEST
DATA BUFFER
READ RESPONSE
DATA BUFFER
READ REQUEST
DEVICE
READ RESPONSE
READ REQUEST
READ RESPONSE

FIG. 4

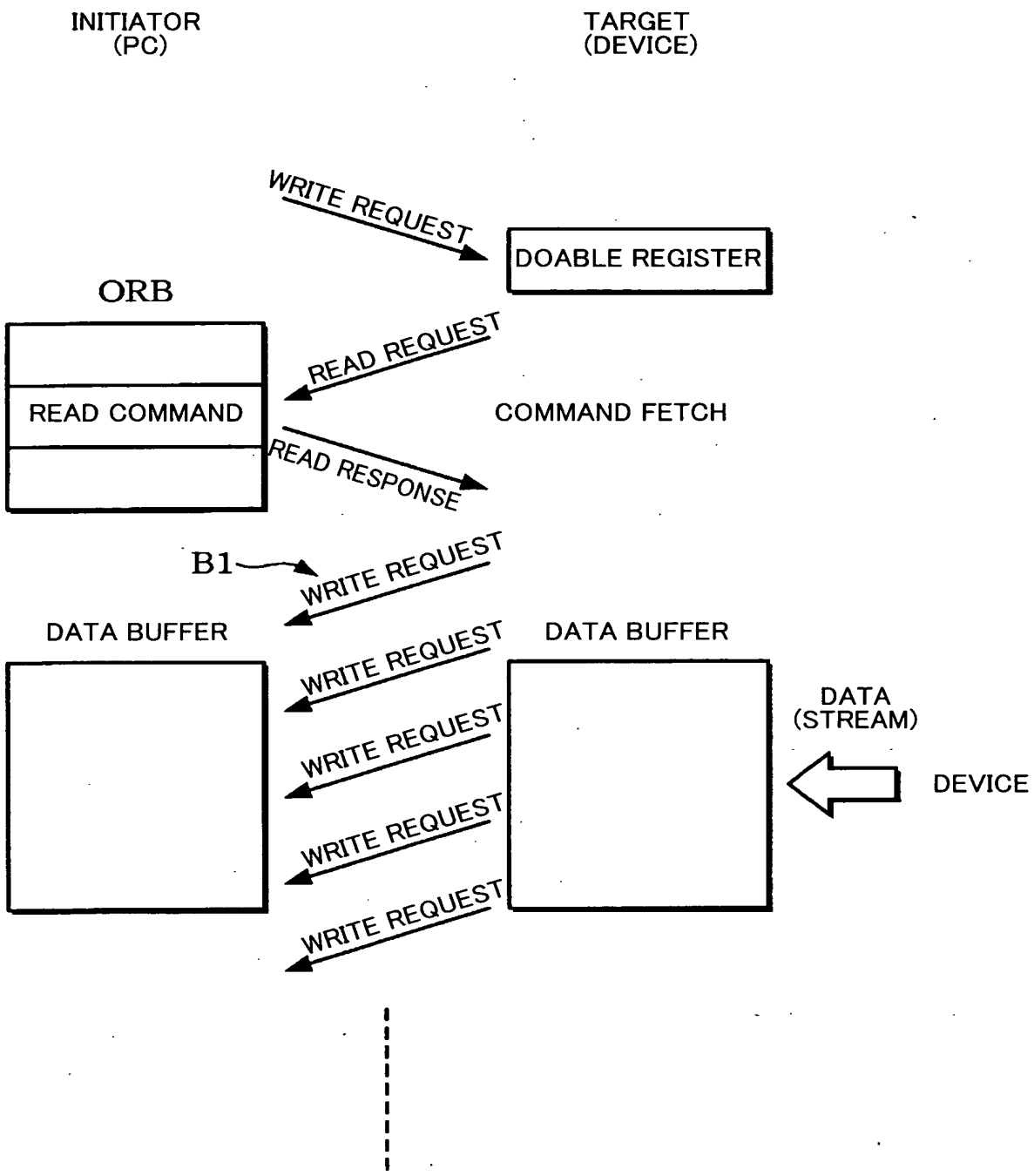

INITIATOR
(PC)
TARGET
(DEVICE)
WRITE REQUEST
DOABLE REGISTER
ORB
READ REQUEST
READ COMMAND
COMMAND FETCH
READ RESPONSE
B1
WRITE REQUEST
DATA BUFFER
DATA BUFFER
WRITE REQUEST
WRITE REQUEST
DATA
(STREAM)
WRITE REQUEST
DEVICE
WRITE REQUEST

FIG. 5A

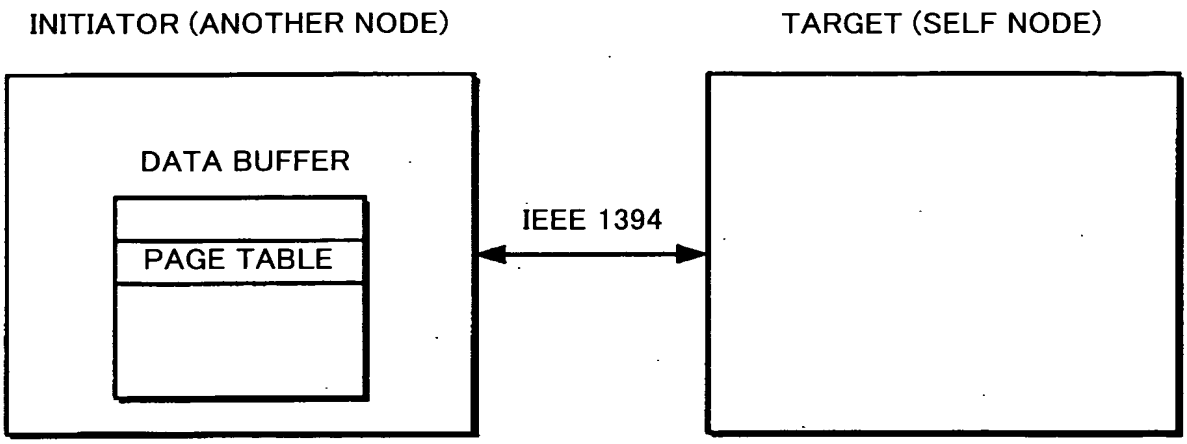


FIG. 5B WHEN PAGE TABLE IS PRESENT

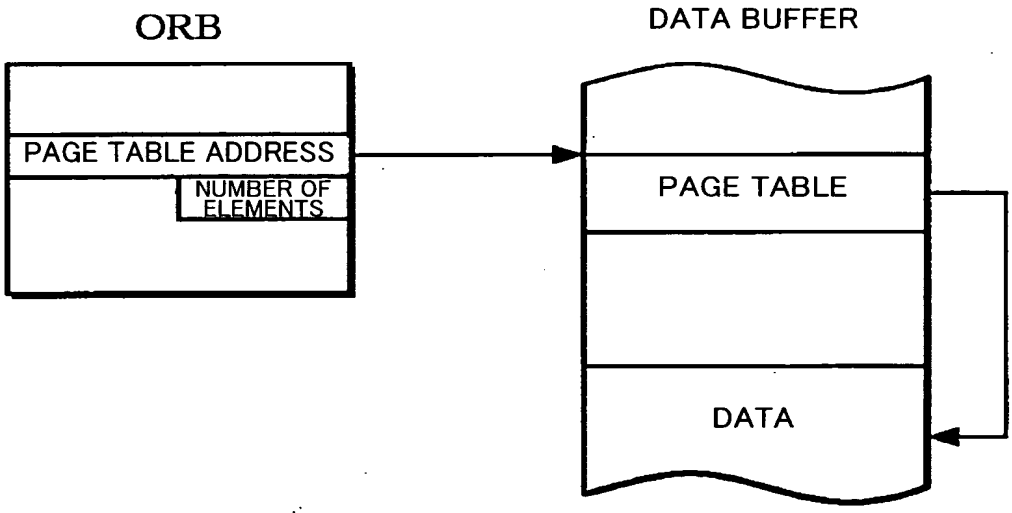


FIG. 5C WHEN PAGE TABLE IS ABSENT

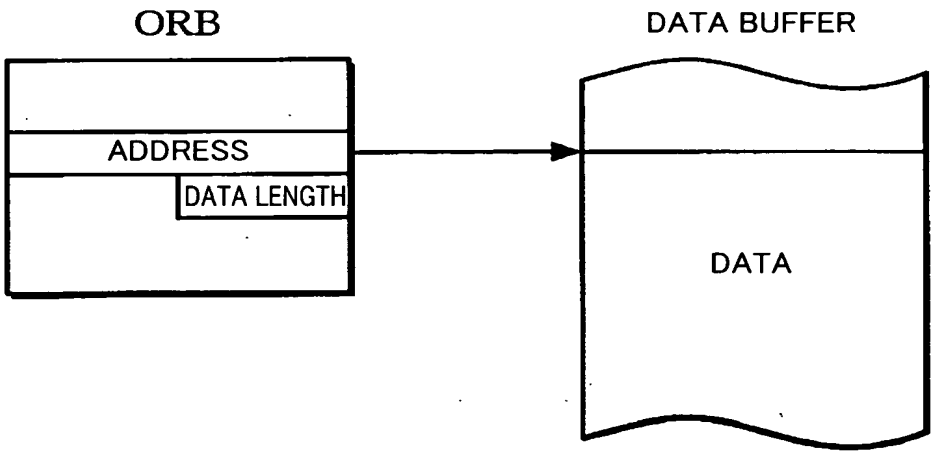


FIG. 6A

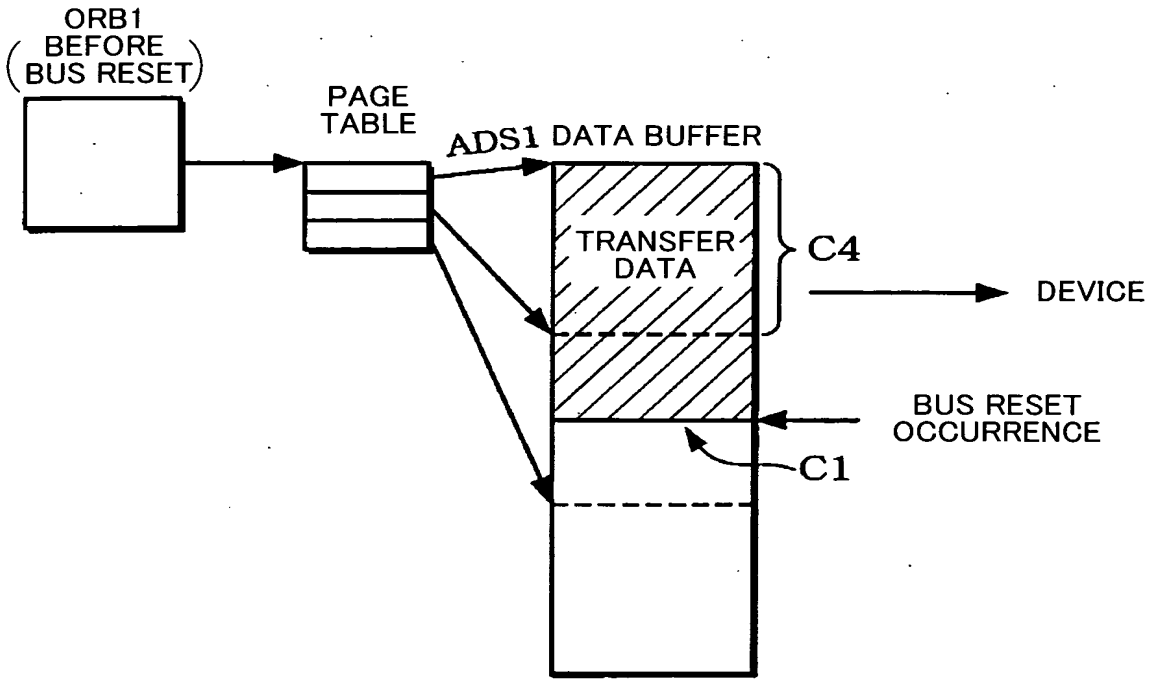

ORB1
(BEFORE
BUS RESET)
PAGE
TABLE
ADS1 DATA BUFFER
TRANSFER
DATA
C4
DEVICE
BUS RESET
OCCURRENCE
C1

FIG. 6B

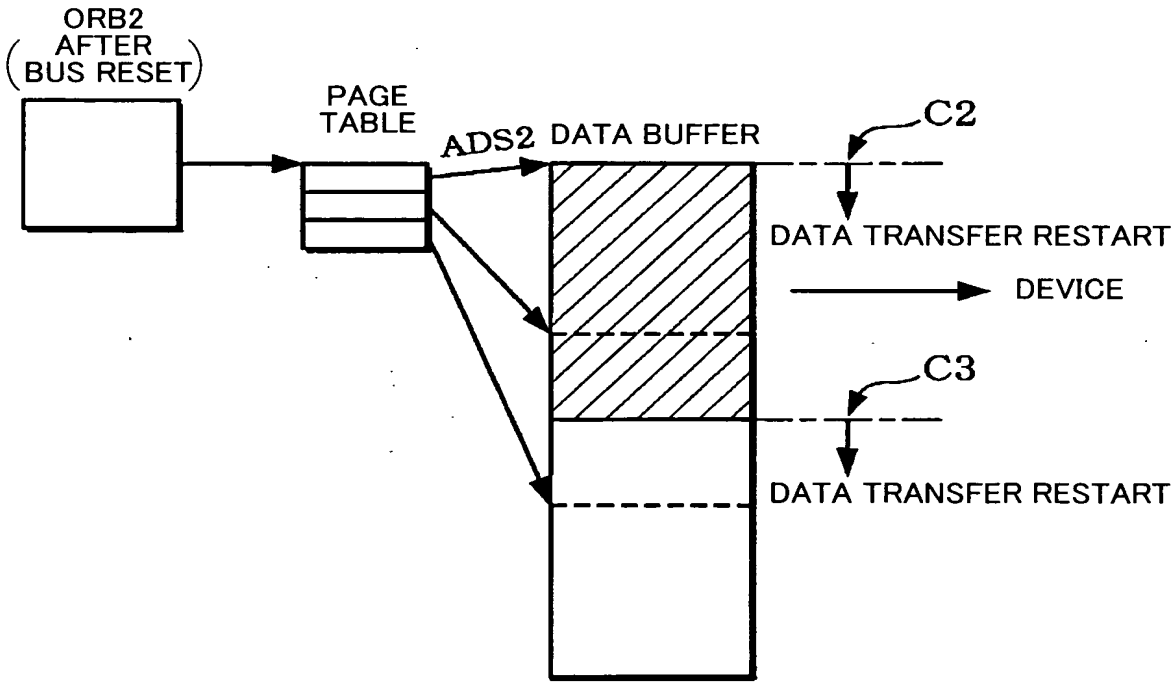

ORB2
(AFTER
BUS RESET)
PAGE
TABLE
ADS2 DATA BUFFER
C2
DATA TRANSFER RESTART
DEVICE
C3
DATA TRANSFER RESTART

FIG. 7

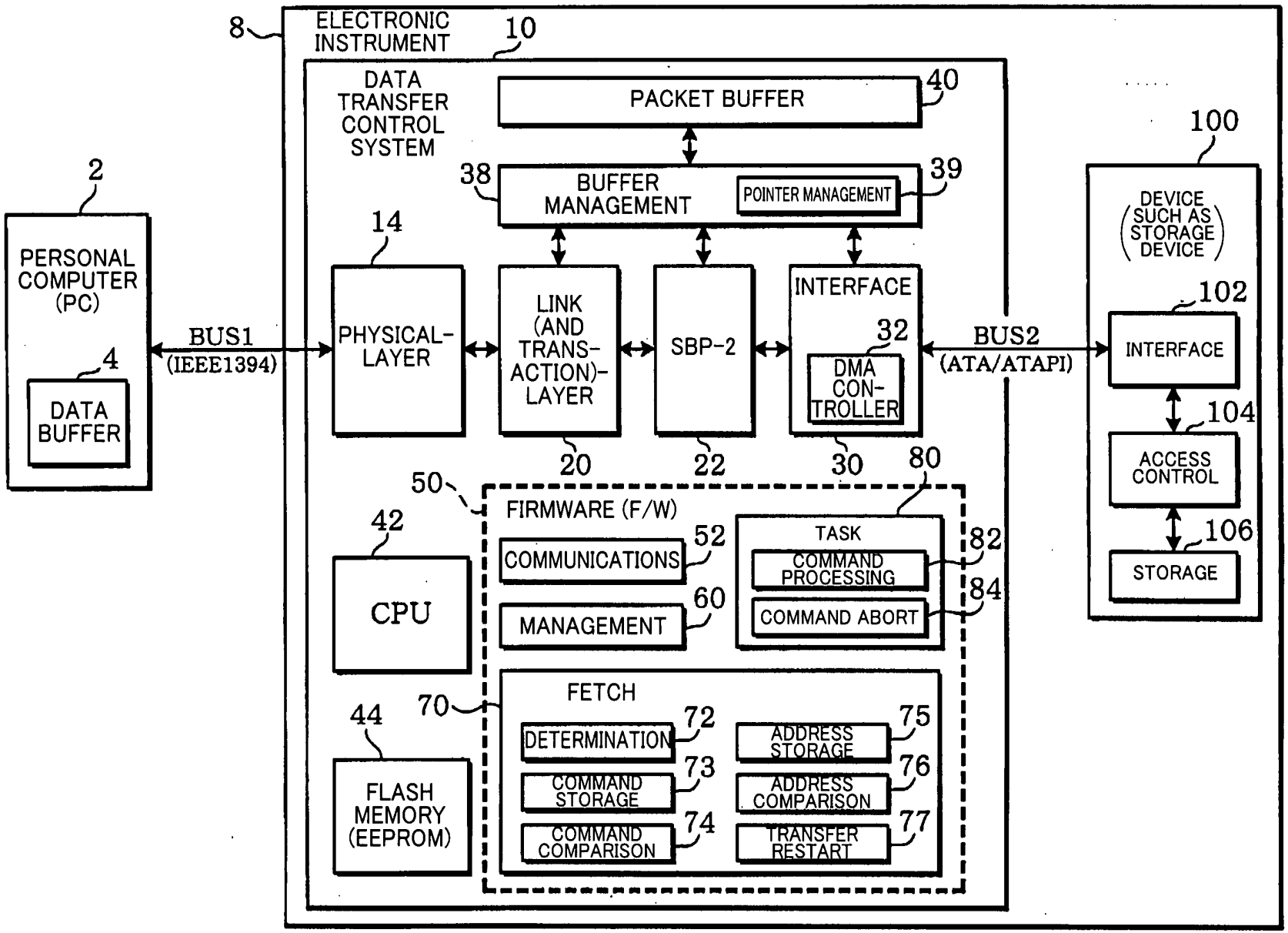

8
ELECTRONIC INSTRUMENT
10
DATA TRANSFER CONTROL SYSTEM
PACKET BUFFER
40
38
BUFFER MANAGEMENT
POINTER MANAGEMENT
39
2
PERSONAL COMPUTER (PC)
4
DATA BUFFER
BUS1 (IEEE1394)
14
PHYSICAL-LAYER
LINK (AND TRANS-ACTION)-LAYER
SBP-2
INTERFACE
32
DMA CON-TROLLER
20
22
30
80
50
FIRMWARE (F/W)
42
CPU
COMMUNICATIONS
52
MANAGEMENT
60
TASK
82
COMMAND PROCESSING
84
COMMAND ABORT
44
FLASH MEMORY (EEPROM)
70
FETCH
DETERMINATION
72
COMMAND STORAGE
73
COMMAND COMPARISON
74
ADDRESS STORAGE
75
ADDRESS COMPARISON
76
TRANSFER RESTART
77
BUS2 (ATA/ATAPI)
100
DEVICE (SUCH AS STORAGE DEVICE)
102
INTERFACE
104
ACCESS CONTROL
106
STORAGE

FIG. 8

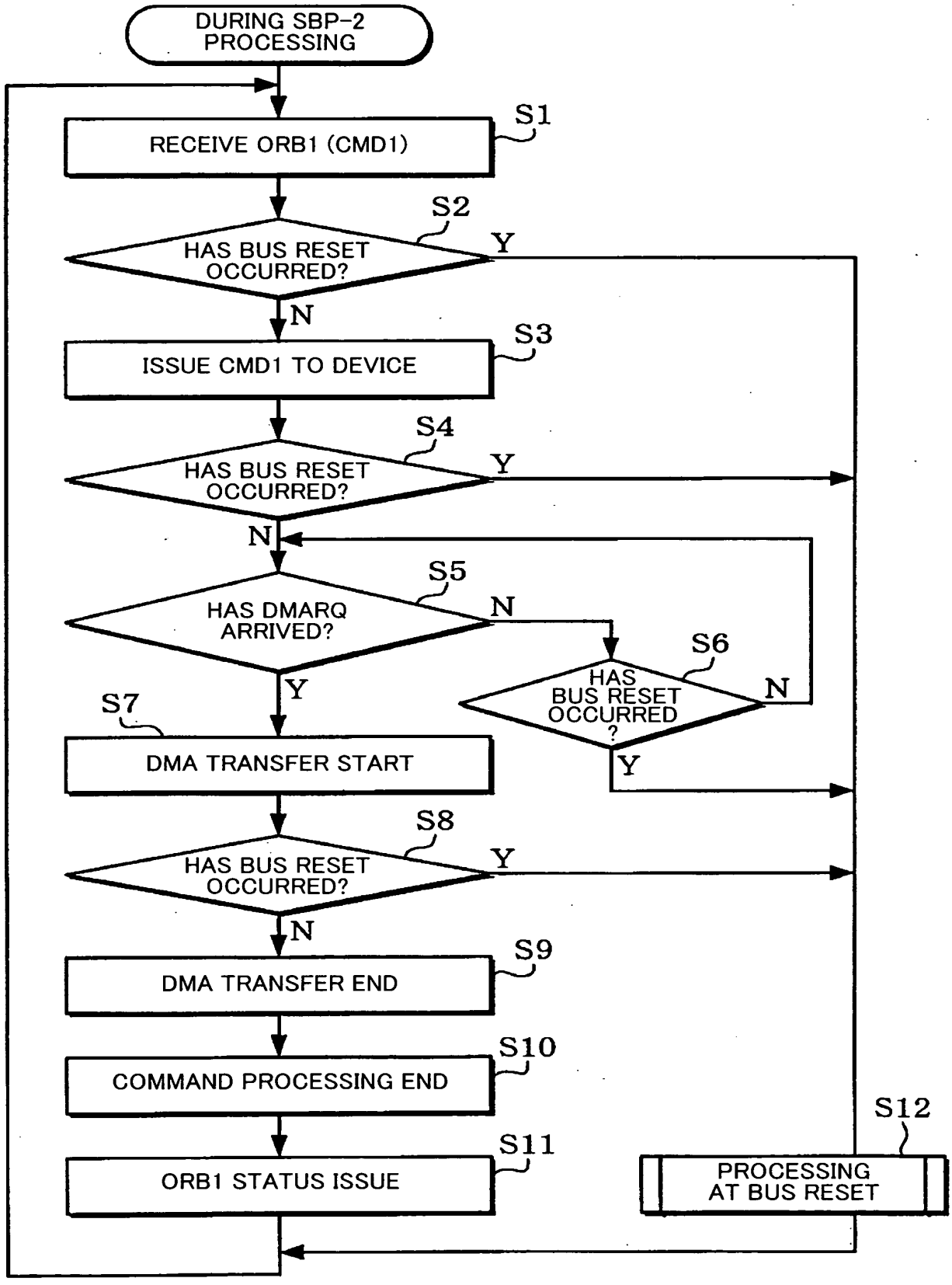

DURING SBP-2 PROCESSING
S1
RECEIVE ORB1 (CMD1)
S2
HAS BUS RESET OCCURRED?
Y
N
S3
ISSUE CMD1 TO DEVICE
S4
HAS BUS RESET OCCURRED?
Y
N
S5
HAS DMARQ ARRIVED?
N
Y
S6
HAS BUS RESET OCCURRED ?
N
Y
S7
DMA TRANSFER START
S8
HAS BUS RESET OCCURRED?
Y
N
S9
DMA TRANSFER END
S10
COMMAND PROCESSING END
S11
ORB1 STATUS ISSUE
S12
PROCESSING AT BUS RESET

FIG. 9

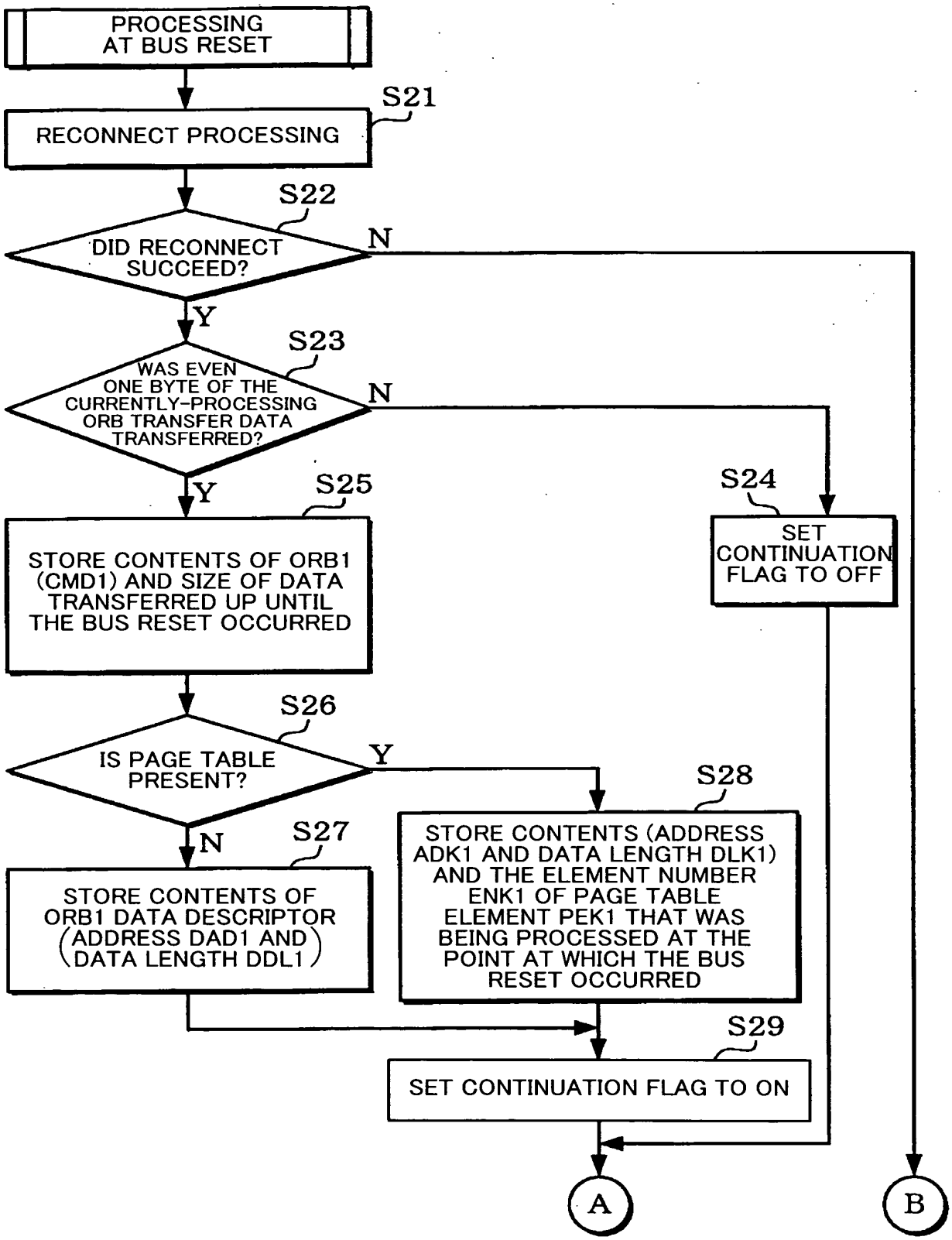

PROCESSING AT BUS RESET
S21
RECONNECT PROCESSING
S22
DID RECONNECT SUCCEED?
N
Y
S23
WAS EVEN ONE BYTE OF THE CURRENTLY-PROCESSING ORB TRANSFER DATA TRANSFERRED?
N
Y
S25
STORE CONTENTS OF ORB1 (CMD1) AND SIZE OF DATA TRANSFERRED UP UNTIL THE BUS RESET OCCURRED
S24
SET CONTINUATION FLAG TO OFF
S26
IS PAGE TABLE PRESENT?
Y
N
S27
STORE CONTENTS OF ORB1 DATA DESCRIPTOR (ADDRESS DAD1 AND DATA LENGTH DDL1)
S28
STORE CONTENTS (ADDRESS ADK1 AND DATA LENGTH DLK1) AND THE ELEMENT NUMBER ENK1 OF PAGE TABLE ELEMENT PEK1 THAT WAS BEING PROCESSED AT THE POINT AT WHICH THE BUS RESET OCCURRED
S29
SET CONTINUATION FLAG TO ON
A
B

FIG. 10

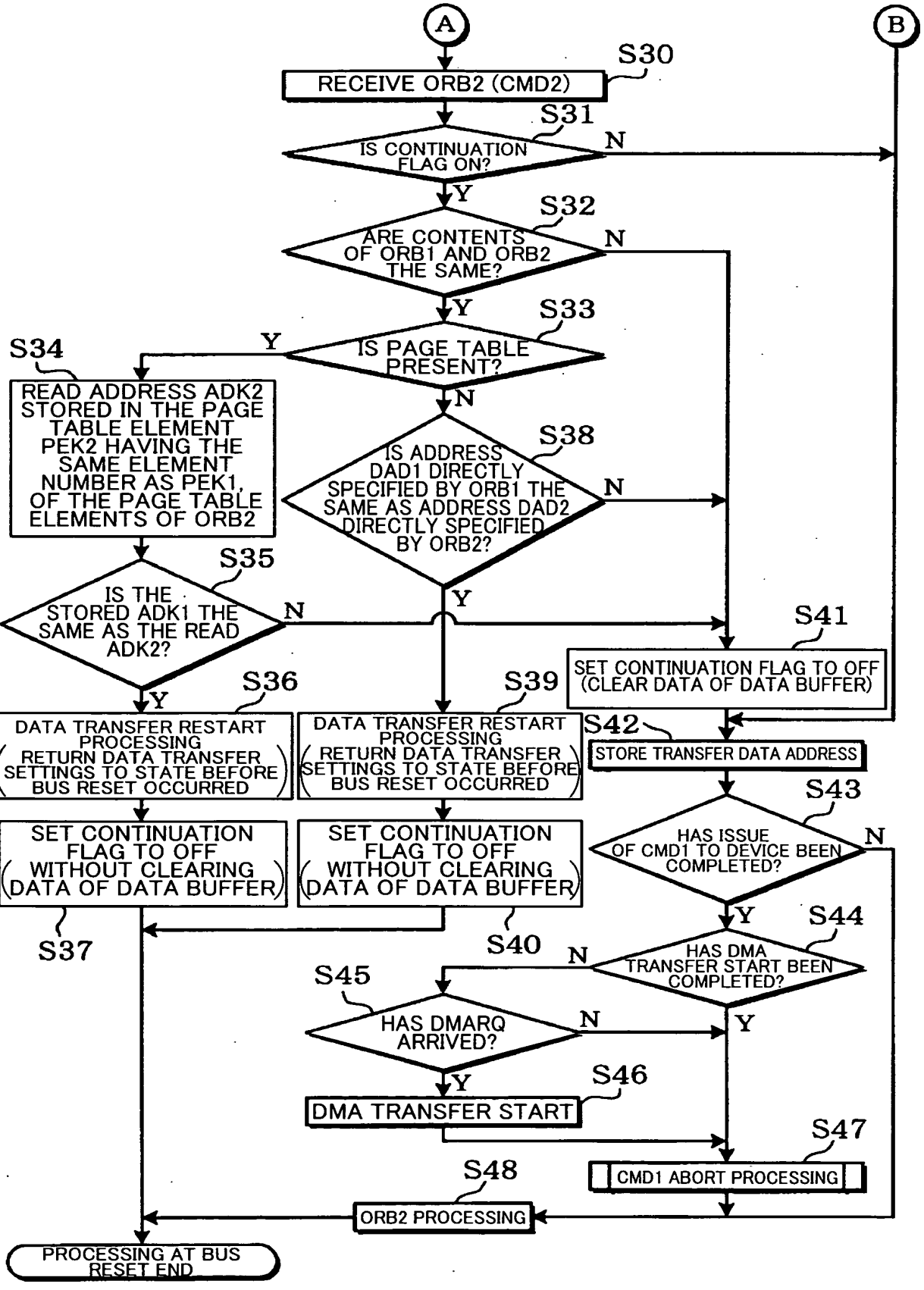

A
B
S30
RECEIVE ORB2 (CMD2)
S31
IS CONTINUATION FLAG ON?
N
Y
S32
ARE CONTENTS OF ORB1 AND ORB2 THE SAME?
N
Y
S33
IS PAGE TABLE PRESENT?
Y
N
S34
READ ADDRESS ADK2 STORED IN THE PAGE TABLE ELEMENT PEK2 HAVING THE SAME ELEMENT NUMBER AS PEK1, OF THE PAGE TABLE ELEMENTS OF ORB2
S35
IS THE STORED ADK1 THE SAME AS THE READ ADK2?
N
Y
S36
DATA TRANSFER RESTART PROCESSING (RETURN DATA TRANSFER SETTINGS TO STATE BEFORE BUS RESET OCCURRED)
S37
SET CONTINUATION FLAG TO OFF WITHOUT CLEARING DATA OF DATA BUFFER
S38
IS ADDRESS DAD1 DIRECTLY SPECIFIED BY ORB1 THE SAME AS ADDRESS DAD2 DIRECTLY SPECIFIED BY ORB2?
N
Y
S39
DATA TRANSFER RESTART PROCESSING (RETURN DATA TRANSFER SETTINGS TO STATE BEFORE BUS RESET OCCURRED)
S40
SET CONTINUATION FLAG TO OFF WITHOUT CLEARING DATA OF DATA BUFFER
S41
SET CONTINUATION FLAG TO OFF (CLEAR DATA OF DATA BUFFER)
S42
STORE TRANSFER DATA ADDRESS
S43
HAS ISSUE OF CMD1 TO DEVICE BEEN COMPLETED?
N
Y
S44
HAS DMA TRANSFER START BEEN COMPLETED?
N
Y
S45
HAS DMARQ ARRIVED?
N
Y
S46
DMA TRANSFER START
S47
CMD1 ABORT PROCESSING
S48
ORB2 PROCESSING
PROCESSING AT BUS RESET END

FIG. 11

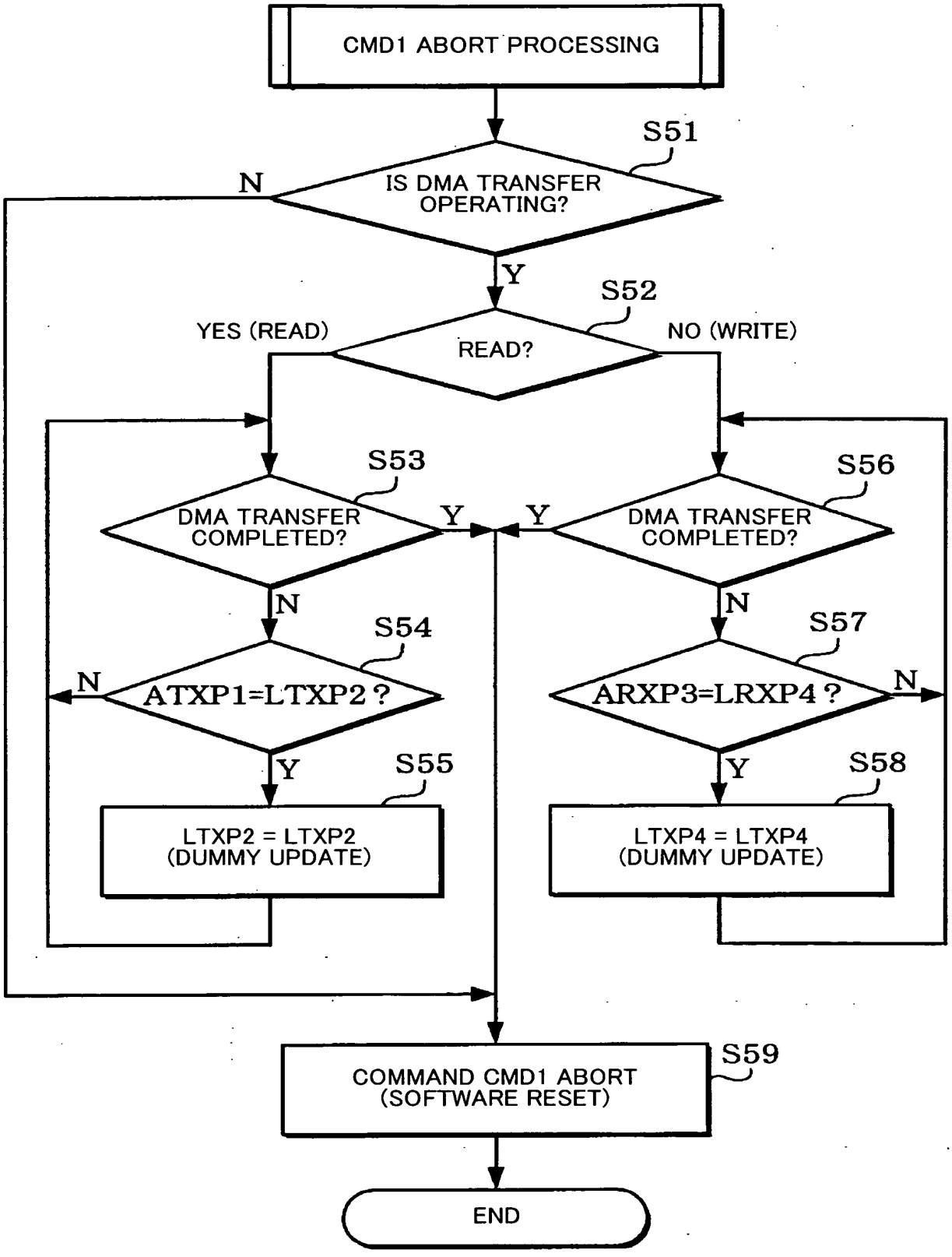

CMD1 ABORT PROCESSING
S51
IS DMA TRANSFER OPERATING?
N
Y
S52
READ?
YES (READ)
NO (WRITE)
S53
DMA TRANSFER COMPLETED?
Y
N
S54
ATXP1=LTXP2 ?
N
Y
S55
LTXP2 = LTXP2 (DUMMY UPDATE)
S56
DMA TRANSFER COMPLETED?
Y
N
S57
ARXP3=LRXP4 ?
N
Y
S58
LTXP4 = LTXP4 (DUMMY UPDATE)
S59
COMMAND CMD1 ABORT (SOFTWARE RESET)
END

FIG. 12

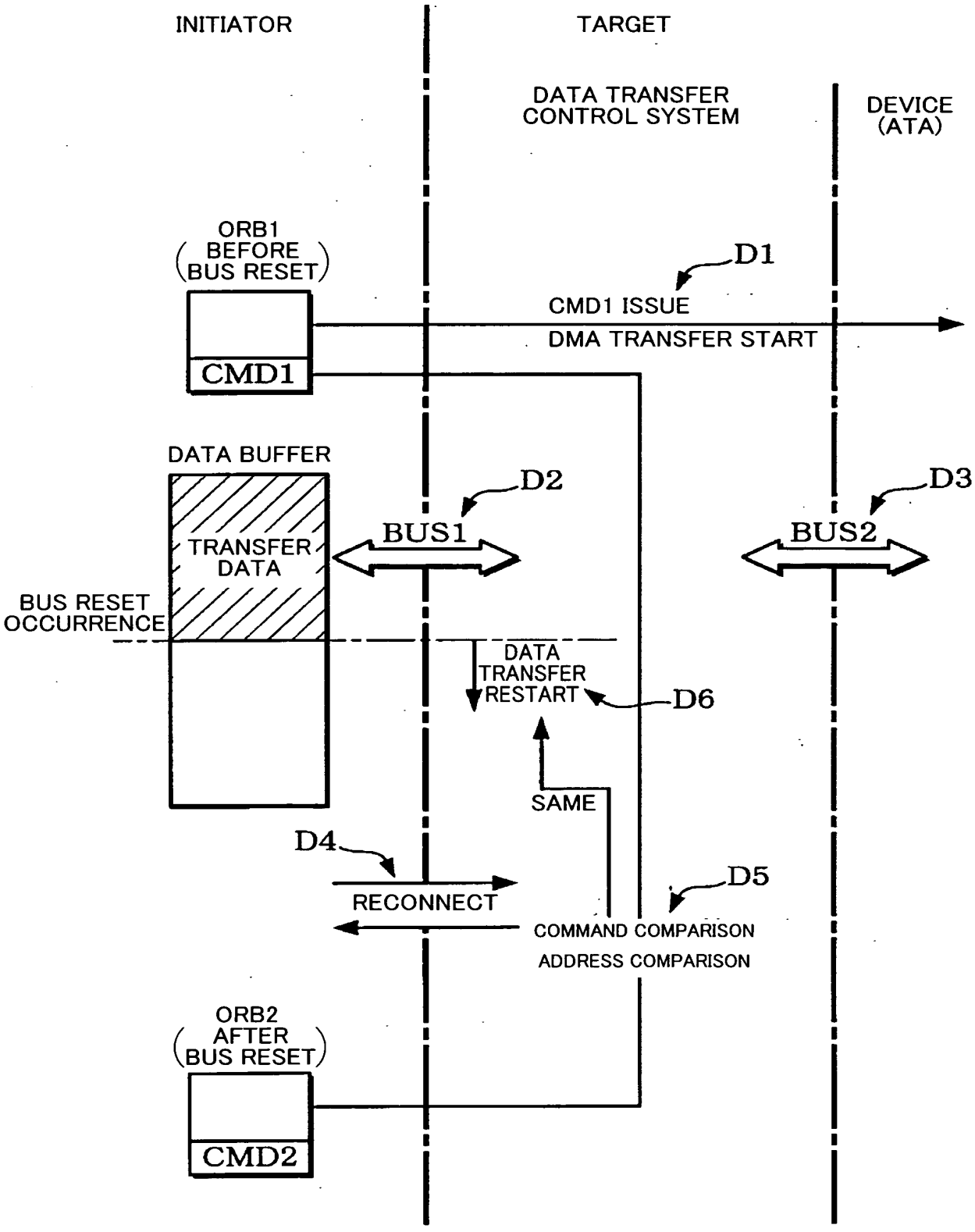

INITIATOR
TARGET
DATA TRANSFER CONTROL SYSTEM
DEVICE (ATA)
ORB1 (BEFORE BUS RESET)
CMD1
D1
CMD1 ISSUE
DMA TRANSFER START
DATA BUFFER
TRANSFER DATA
D2
BUS1
D3
BUS2
BUS RESET OCCURRENCE
DATA TRANSFER RESTART
D6
SAME
D4
RECONNECT
D5
COMMAND COMPARISON
ADDRESS COMPARISON
ORB2 (AFTER BUS RESET)
CMD2

FIG. 13

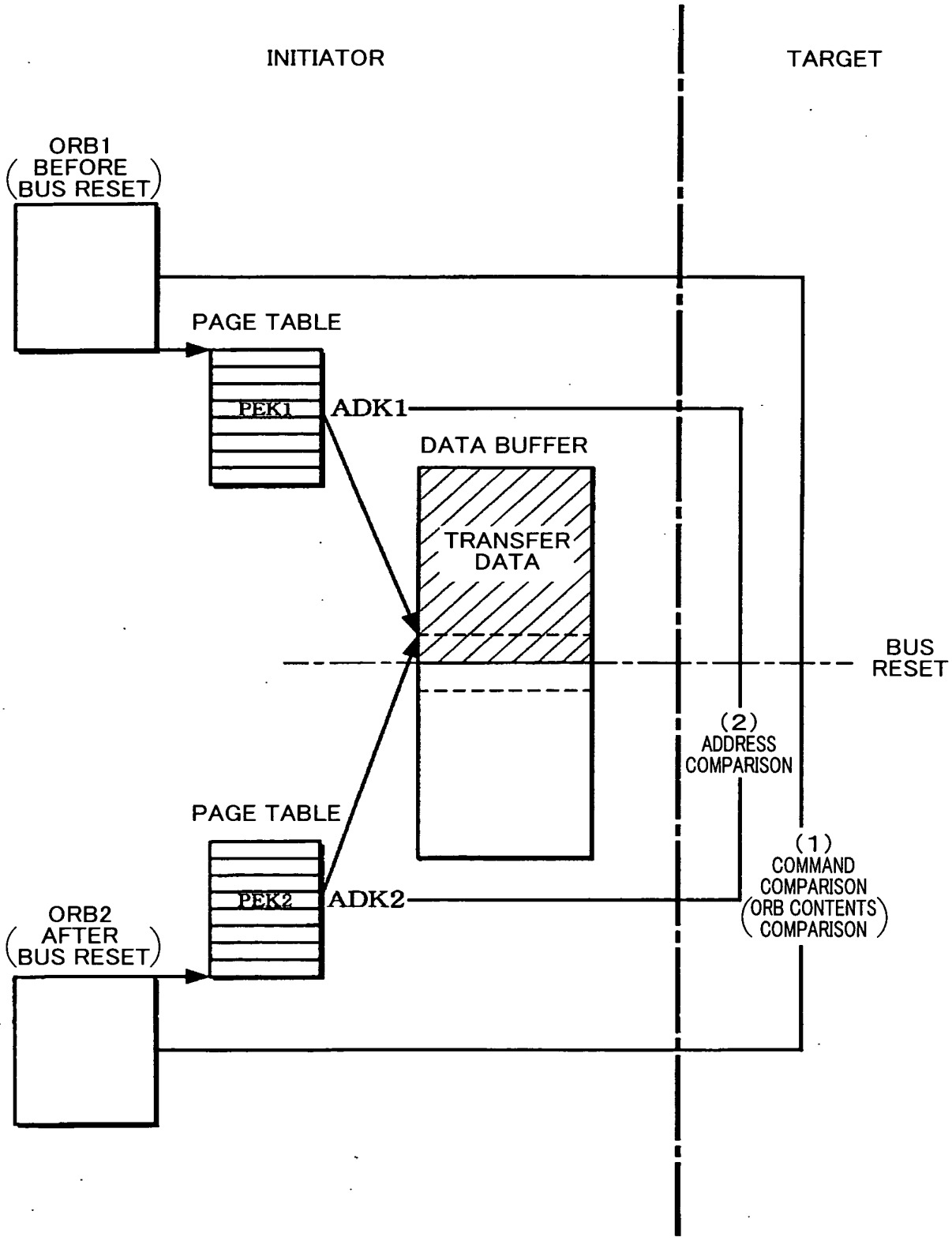

INITIATOR
TARGET
ORB1
(BEFORE
BUS RESET)
PAGE TABLE
PEK1
ADK1
DATA BUFFER
TRANSFER
DATA
BUS
RESET
(2)
ADDRESS
COMPARISON
PAGE TABLE
(1)
COMMAND
COMPARISON
(ORB CONTENTS
COMPARISON)
PEK2
ADK2
ORB2
(AFTER
BUS RESET)

FIG. 14

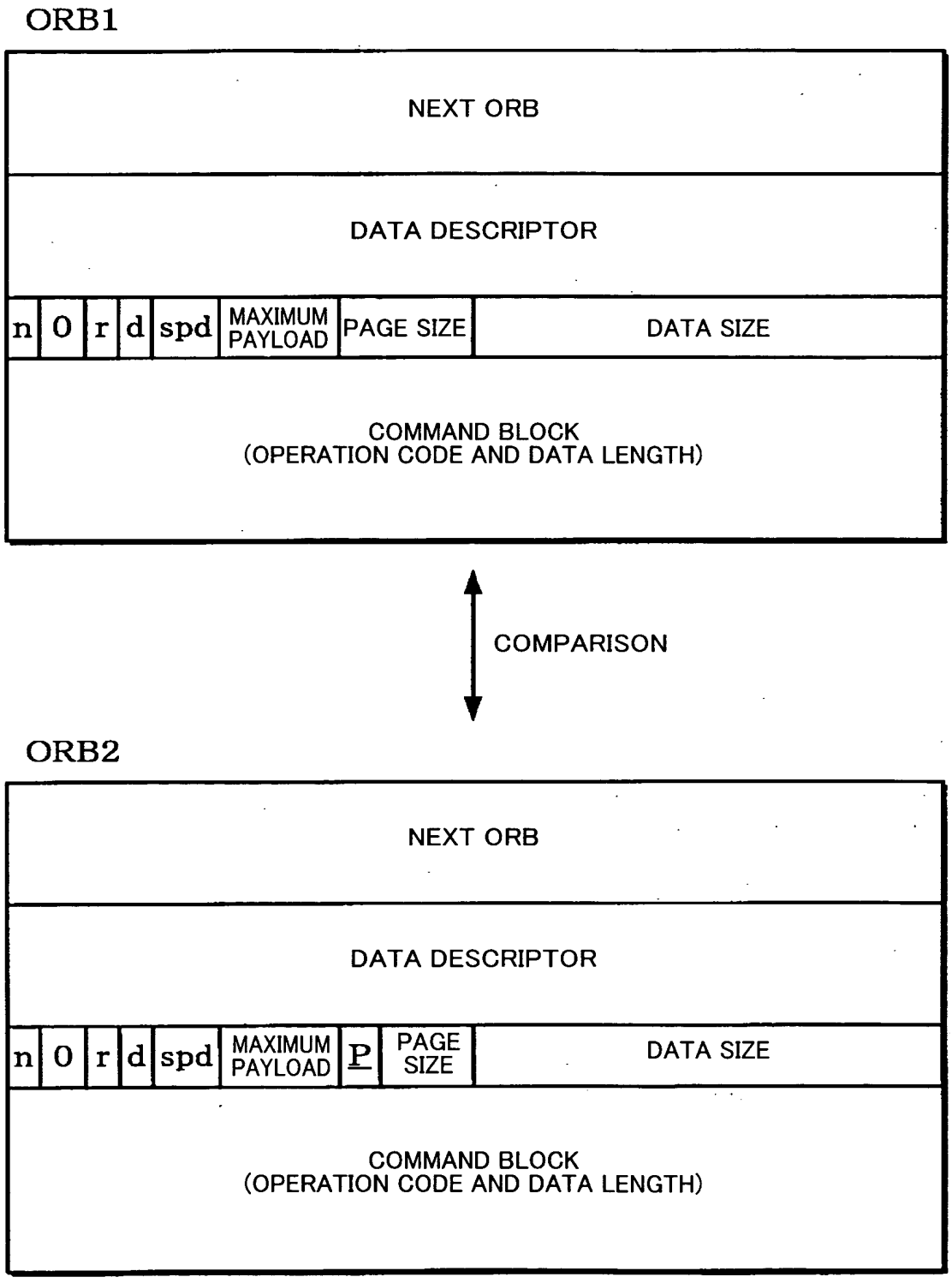

ORB1
NEXT ORB
DATA DESCRIPTOR
n
0
r
d
spd
MAXIMUM PAYLOAD
PAGE SIZE
DATA SIZE
COMMAND BLOCK
(OPERATION CODE AND DATA LENGTH)
COMPARISON
ORB2
NEXT ORB
DATA DESCRIPTOR
n
0
r
d
spd
MAXIMUM PAYLOAD
P
PAGE SIZE
DATA SIZE
COMMAND BLOCK
(OPERATION CODE AND DATA LENGTH)

FIG. 15

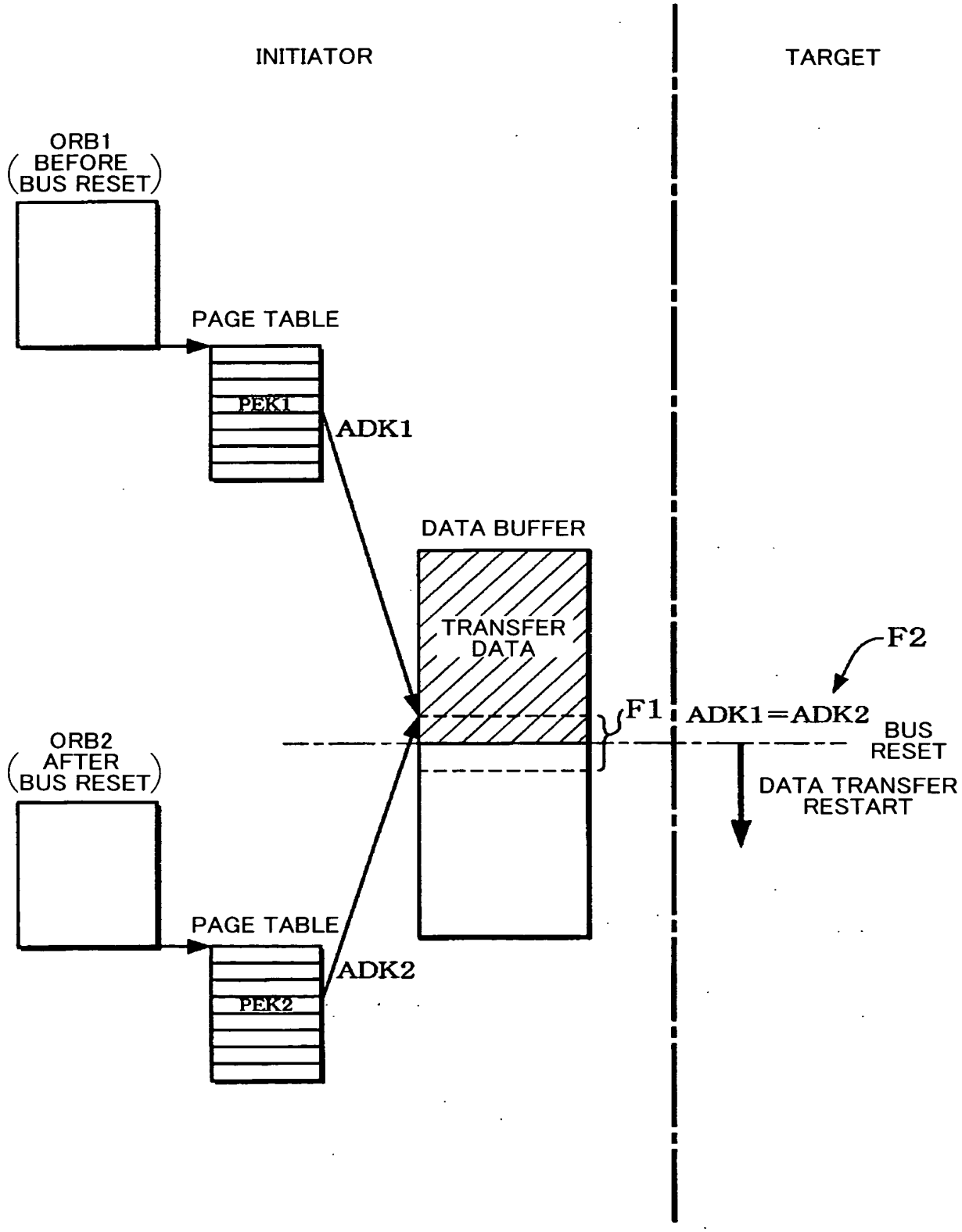

INITIATOR
TARGET
ORB1
(BEFORE
BUS RESET)
PAGE TABLE
PEK1
ADK1
DATA BUFFER
TRANSFER
DATA
F2
F1
ADK1=ADK2
BUS
RESET
DATA TRANSFER
RESTART
ORB2
(AFTER
BUS RESET)
PAGE TABLE
ADK2
PEK2

FIG. 16

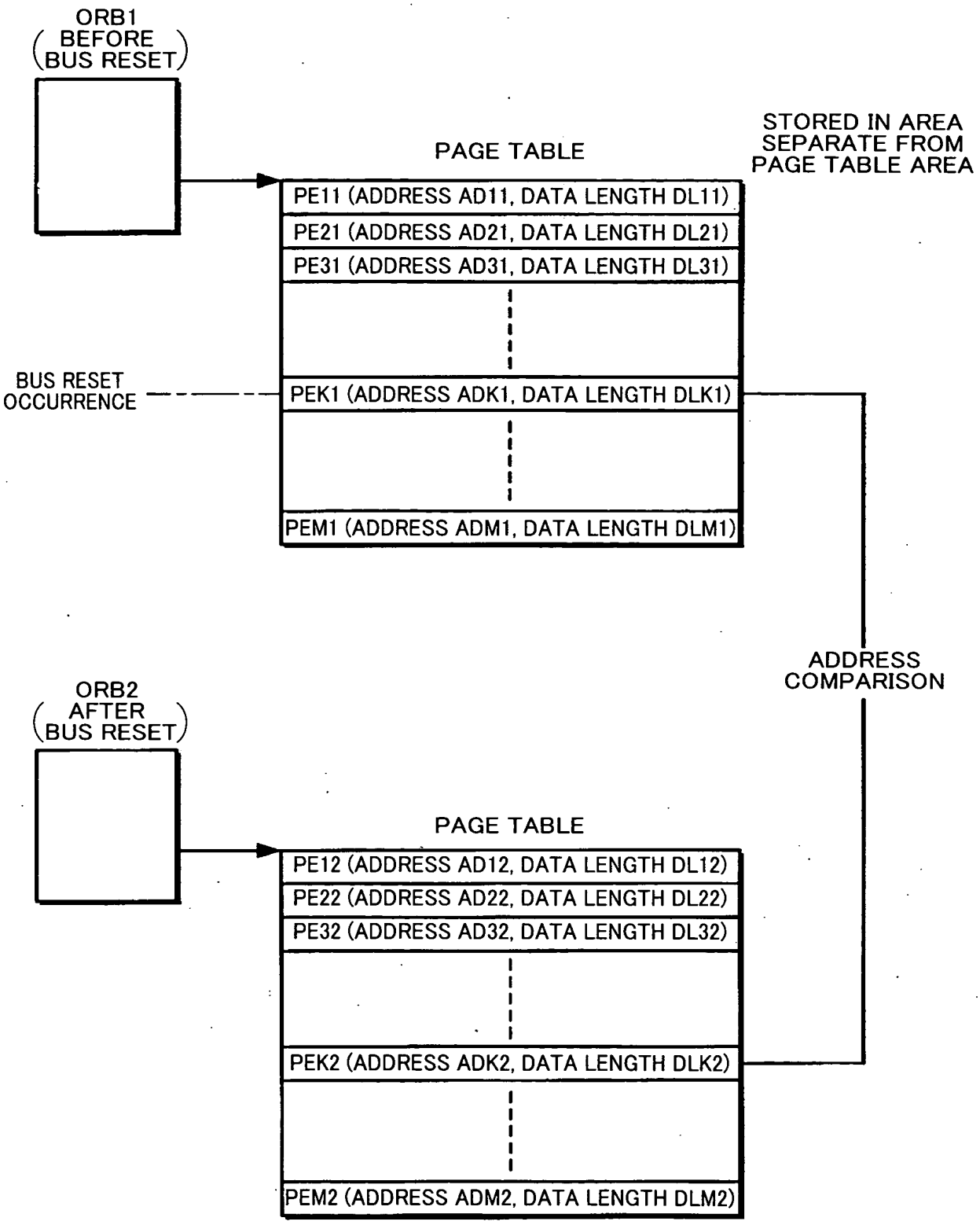

ORB1
(BEFORE BUS RESET)
PAGE TABLE
STORED IN AREA SEPARATE FROM PAGE TABLE AREA
PE11 (ADDRESS AD11, DATA LENGTH DL11)
PE21 (ADDRESS AD21, DATA LENGTH DL21)
PE31 (ADDRESS AD31, DATA LENGTH DL31)
BUS RESET OCCURRENCE
PEK1 (ADDRESS ADK1, DATA LENGTH DLK1)
PEM1 (ADDRESS ADM1, DATA LENGTH DLM1)
ADDRESS COMPARISON
ORB2
(AFTER BUS RESET)
PAGE TABLE
PE12 (ADDRESS AD12, DATA LENGTH DL12)
PE22 (ADDRESS AD22, DATA LENGTH DL22)
PE32 (ADDRESS AD32, DATA LENGTH DL32)
PEK2 (ADDRESS ADK2, DATA LENGTH DLK2)
PEM2 (ADDRESS ADM2, DATA LENGTH DLM2)

FIG. 17

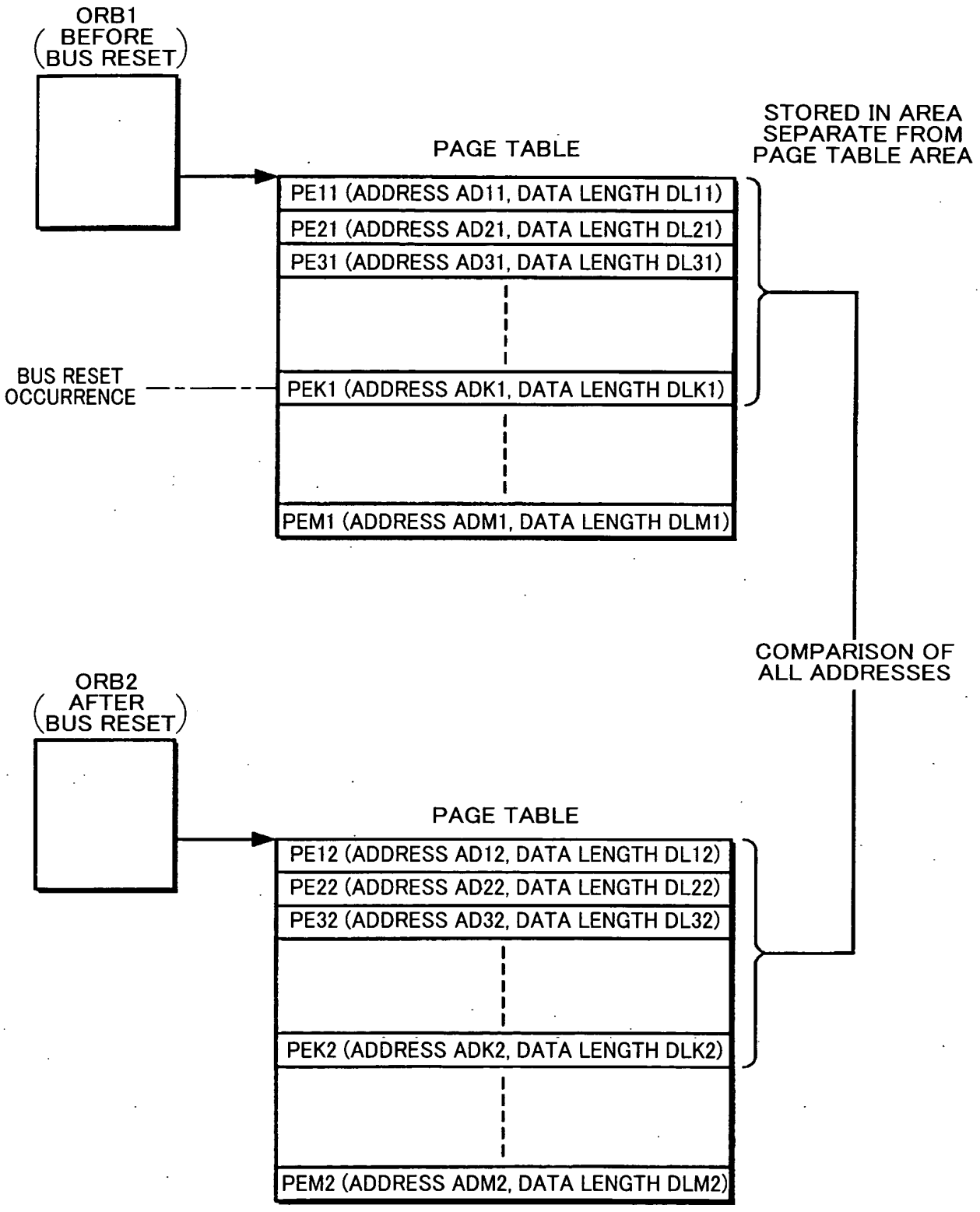

ORB1
(BEFORE BUS RESET)
PAGE TABLE
STORED IN AREA SEPARATE FROM PAGE TABLE AREA
PE11 (ADDRESS AD11, DATA LENGTH DL11)
PE21 (ADDRESS AD21, DATA LENGTH DL21)
PE31 (ADDRESS AD31, DATA LENGTH DL31)
BUS RESET OCCURRENCE
PEK1 (ADDRESS ADK1, DATA LENGTH DLK1)
PEM1 (ADDRESS ADM1, DATA LENGTH DLM1)
COMPARISON OF ALL ADDRESSES
ORB2
(AFTER BUS RESET)
PAGE TABLE
PE12 (ADDRESS AD12, DATA LENGTH DL12)
PE22 (ADDRESS AD22, DATA LENGTH DL22)
PE32 (ADDRESS AD32, DATA LENGTH DL32)
PEK2 (ADDRESS ADK2, DATA LENGTH DLK2)
PEM2 (ADDRESS ADM2, DATA LENGTH DLM2)

FIG. 18

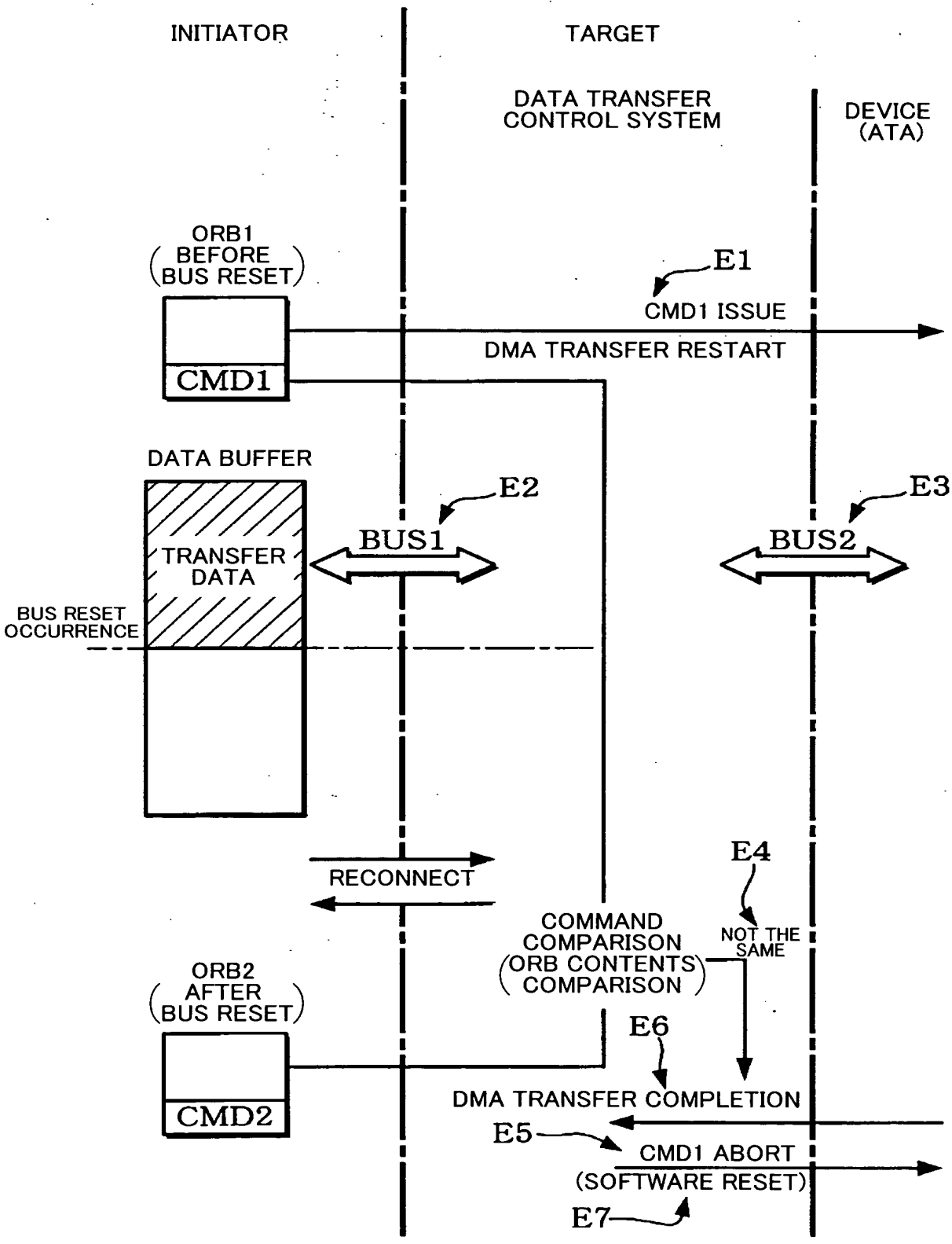

INITIATOR
TARGET
DATA TRANSFER CONTROL SYSTEM
DEVICE (ATA)
ORB1 (BEFORE BUS RESET)
CMD1
E1
CMD1 ISSUE
DMA TRANSFER RESTART
DATA BUFFER
TRANSFER DATA
BUS RESET OCCURRENCE
E2
BUS1
E3
BUS2
RECONNECT
E4
COMMAND COMPARISON (ORB CONTENTS COMPARISON)
NOT THE SAME
ORB2 (AFTER BUS RESET)
CMD2
E6
DMA TRANSFER COMPLETION
E5
CMD1 ABORT (SOFTWARE RESET)
E7

FIG. 19A

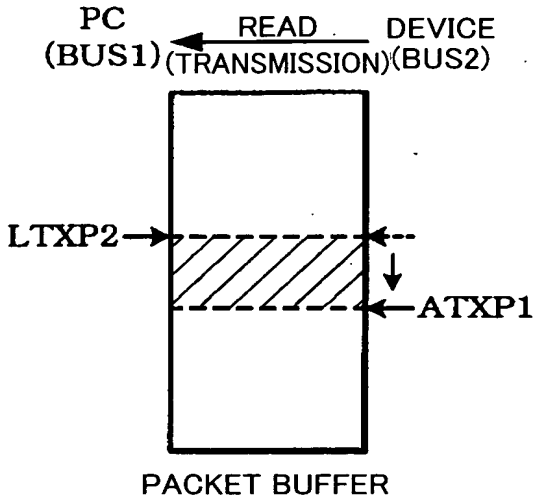


FIG. 19B

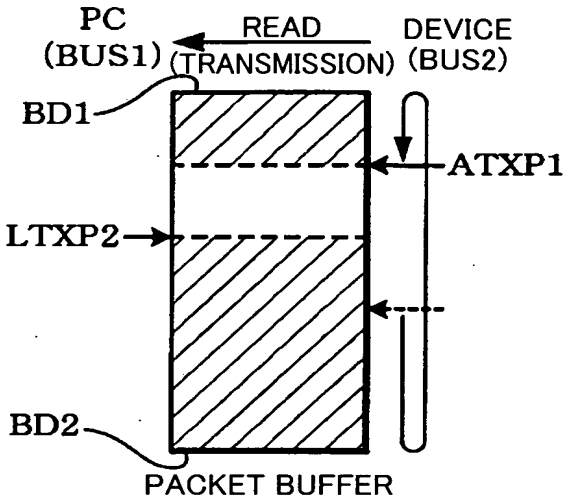


FIG. 19C

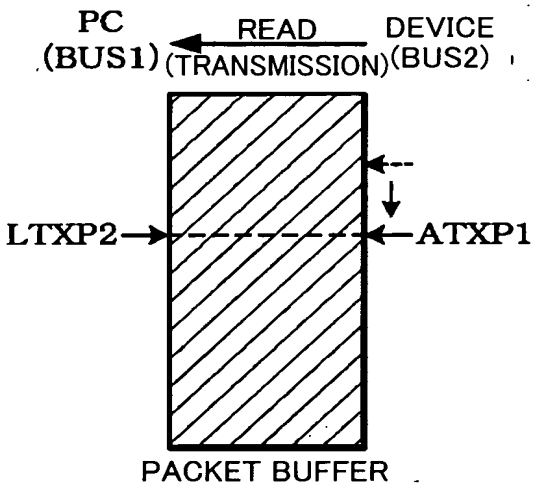


FIG. 19D

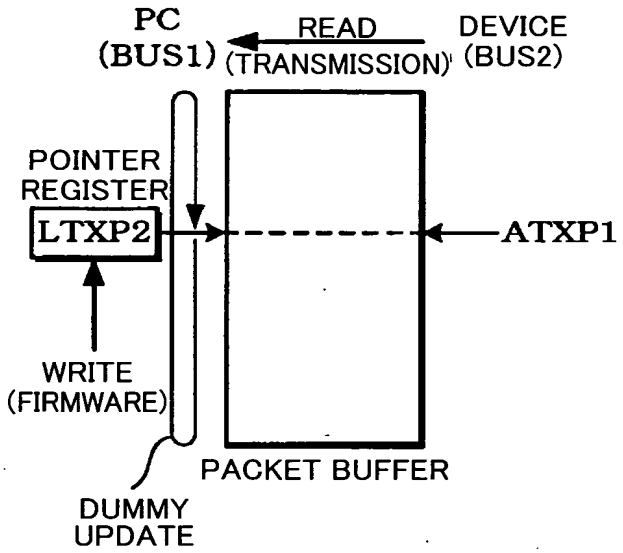


FIG. 19E

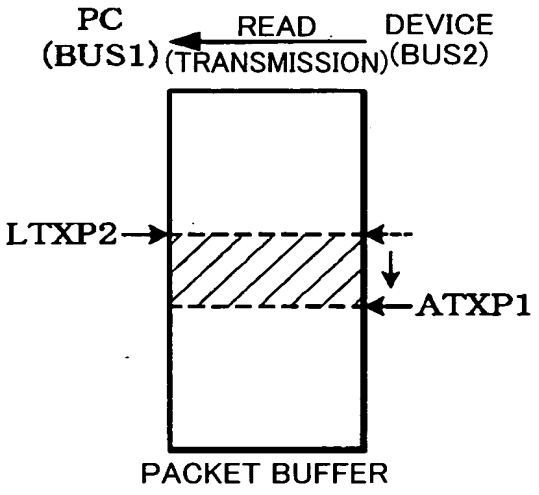


FIG. 20A

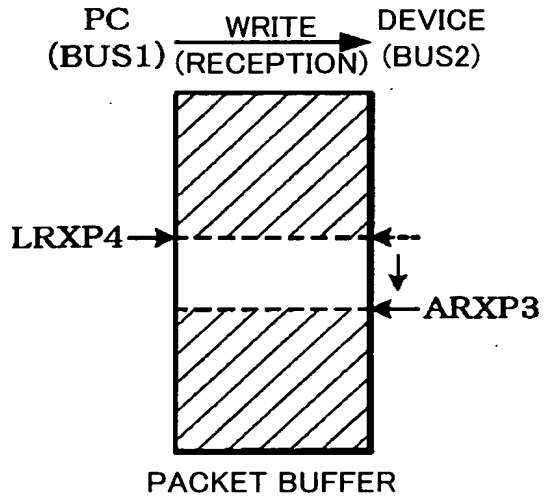


FIG. 20B

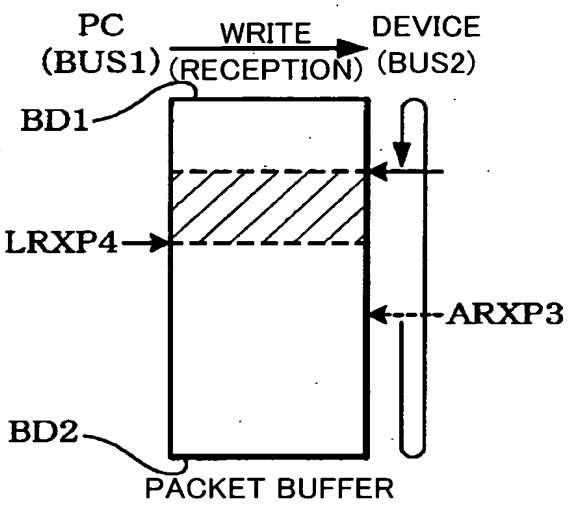


FIG. 20C

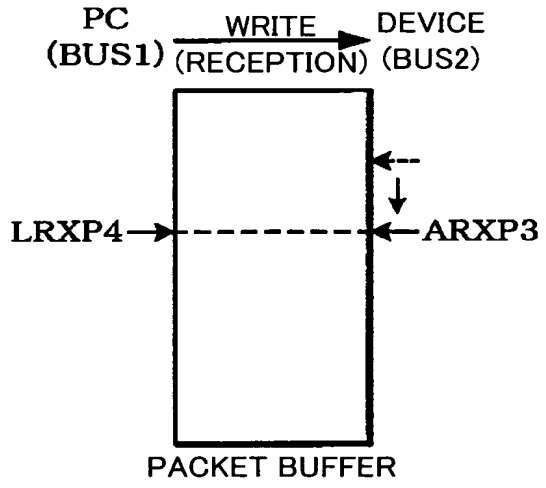


FIG. 20D

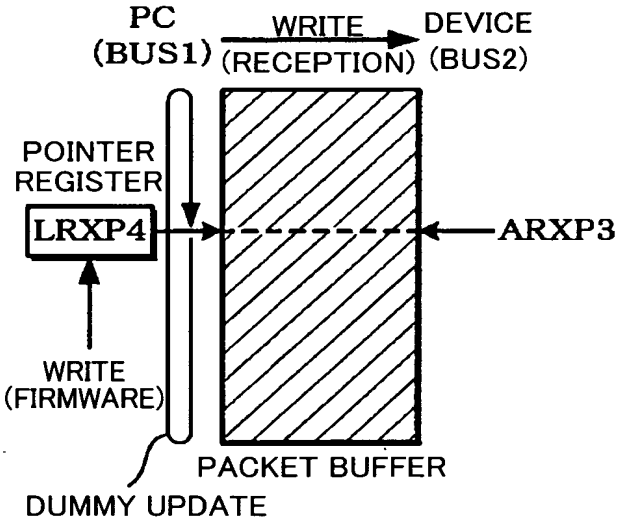


FIG. 20E

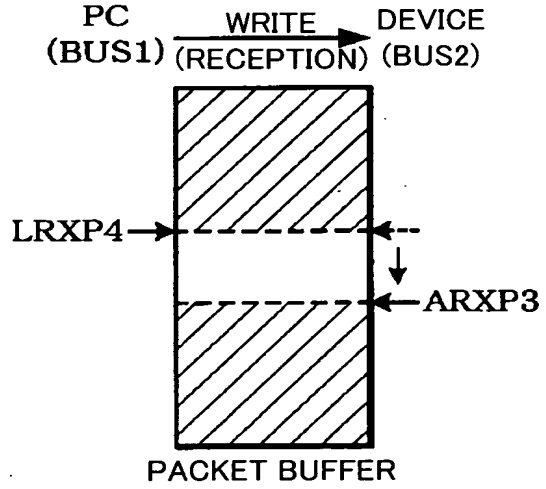


FIG. 21

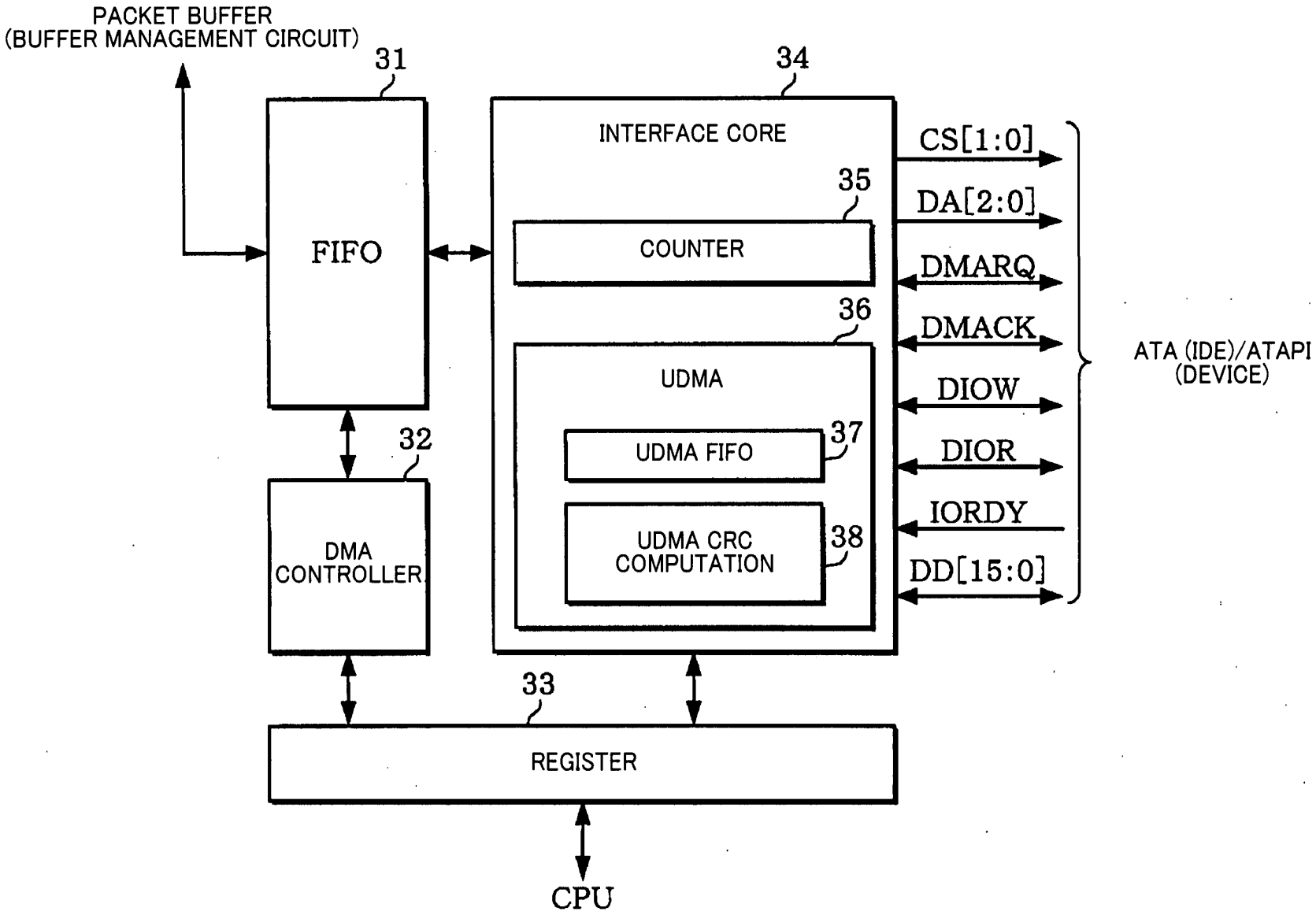

PACKET BUFFER
(BUFFER MANAGEMENT CIRCUIT)
31
34
FIFO
INTERFACE CORE
35
COUNTER
36
UDMA
37
UDMA FIFO
38
UDMA CRC
COMPUTATION
32
DMA
CONTROLLER
33
REGISTER
CPU
CS[1:0]
DA[2:0]
DMARQ
DMACK
DIOW
DIOR
IORDY
DD[15:0]
ATA (IDE)/ATAPI
(DEVICE)

FIG. 22A PIO READ (DEVICE --> DATA TRANSFER CONTROL SYSTEM --> PC)

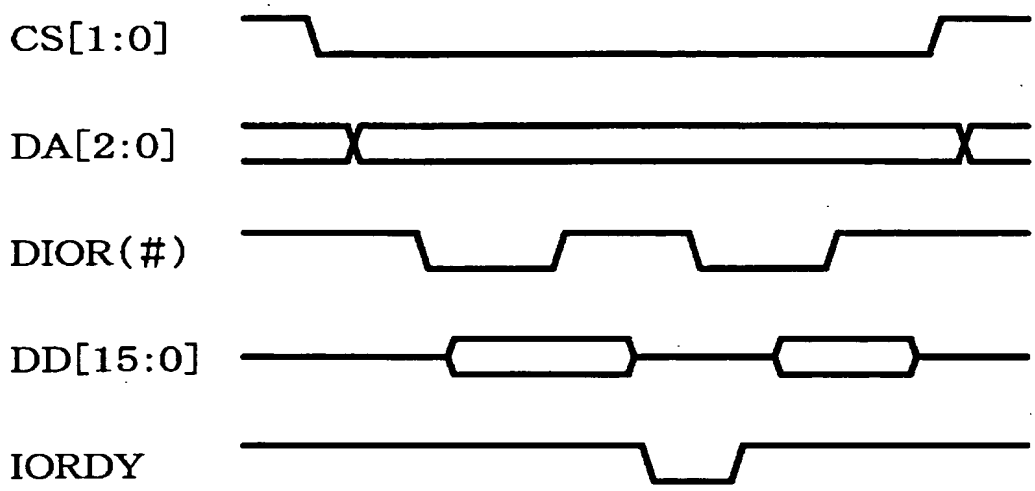


FIG. 22B PIO WRITE (PC --> DATA TRANSFER CONTROL SYSTEM --> DEVICE)

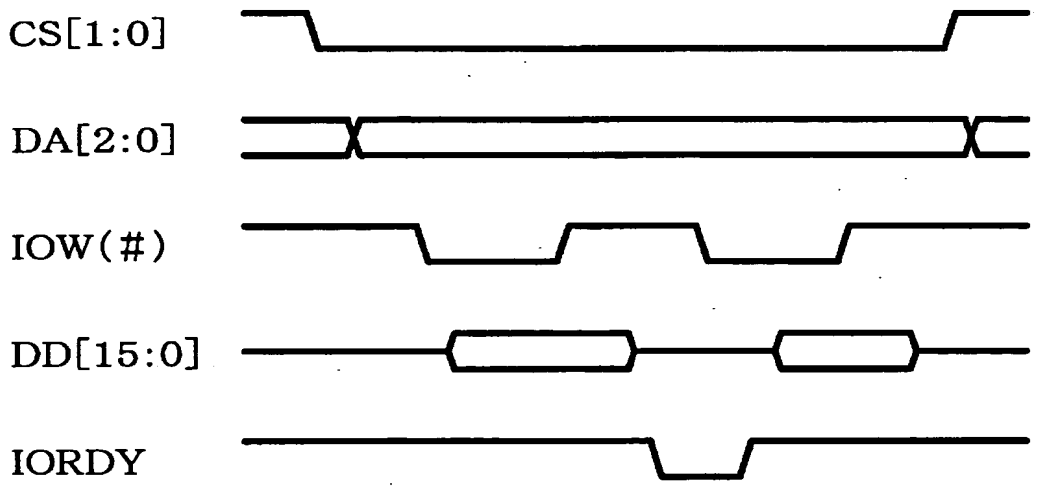


FIG. 23A DMA READ (DEVICE --> DATA TRANSFER CONTROL SYSTEM --> PC)

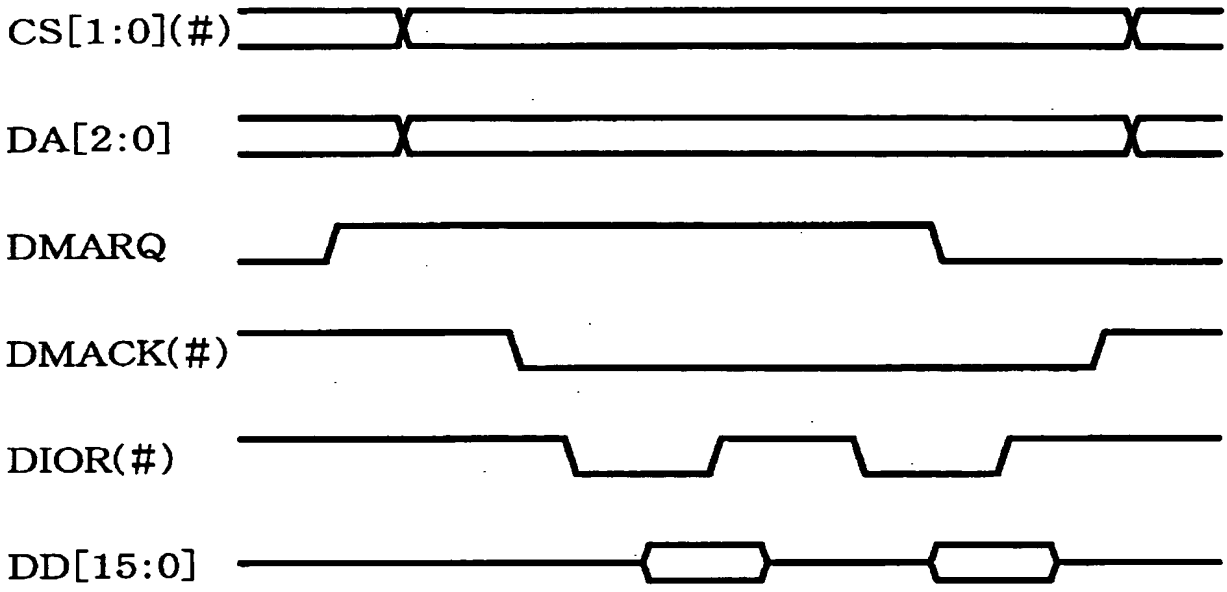


FIG. 23B DMA WRITE (PC --> DATA TRANSFER CONTROL SYSTEM --> DEVICE)

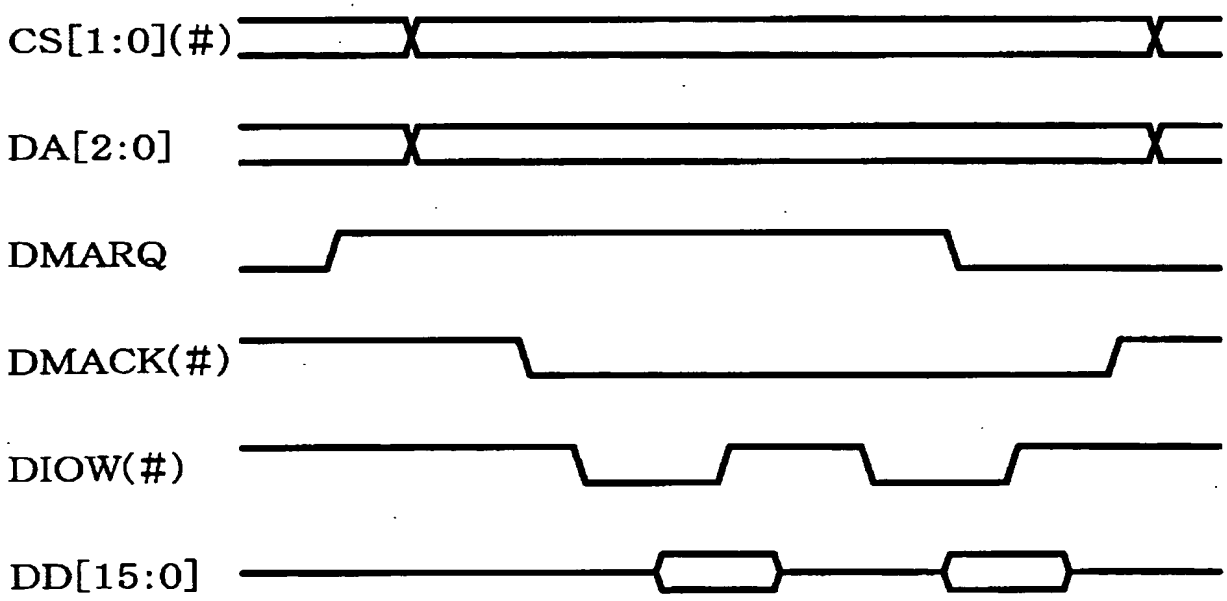


FIG. 24A

ULTRA-DMA READ (DEVICE --> DATA TRANSFER CONTROL SYSTEM --> PC)

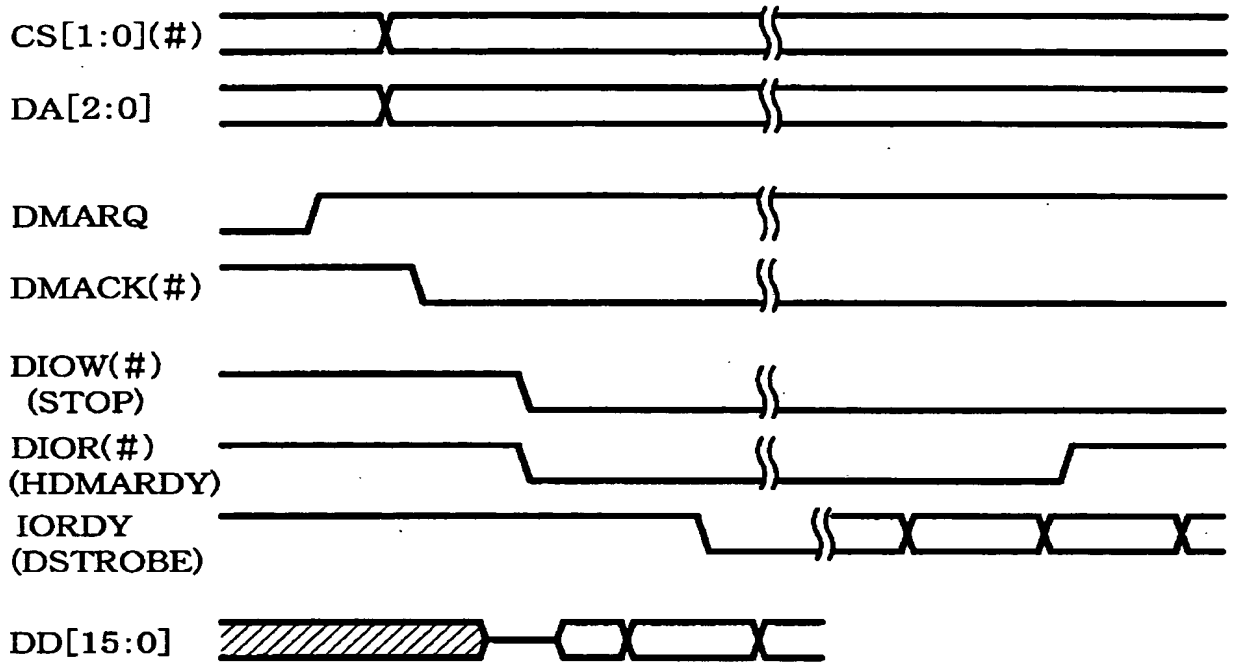


FIG. 24B

ULTRA-DMA WRITE (PC --> DATA TRANSFER CONTROL SYSTEM --> DEVICE)

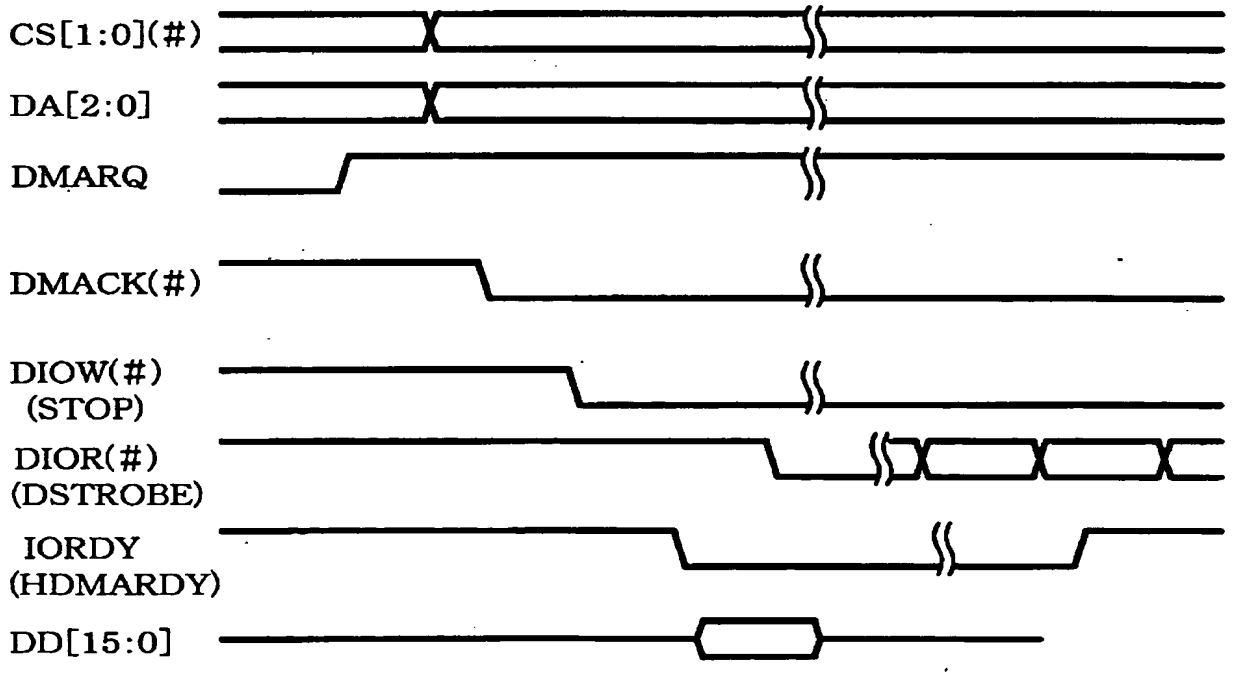
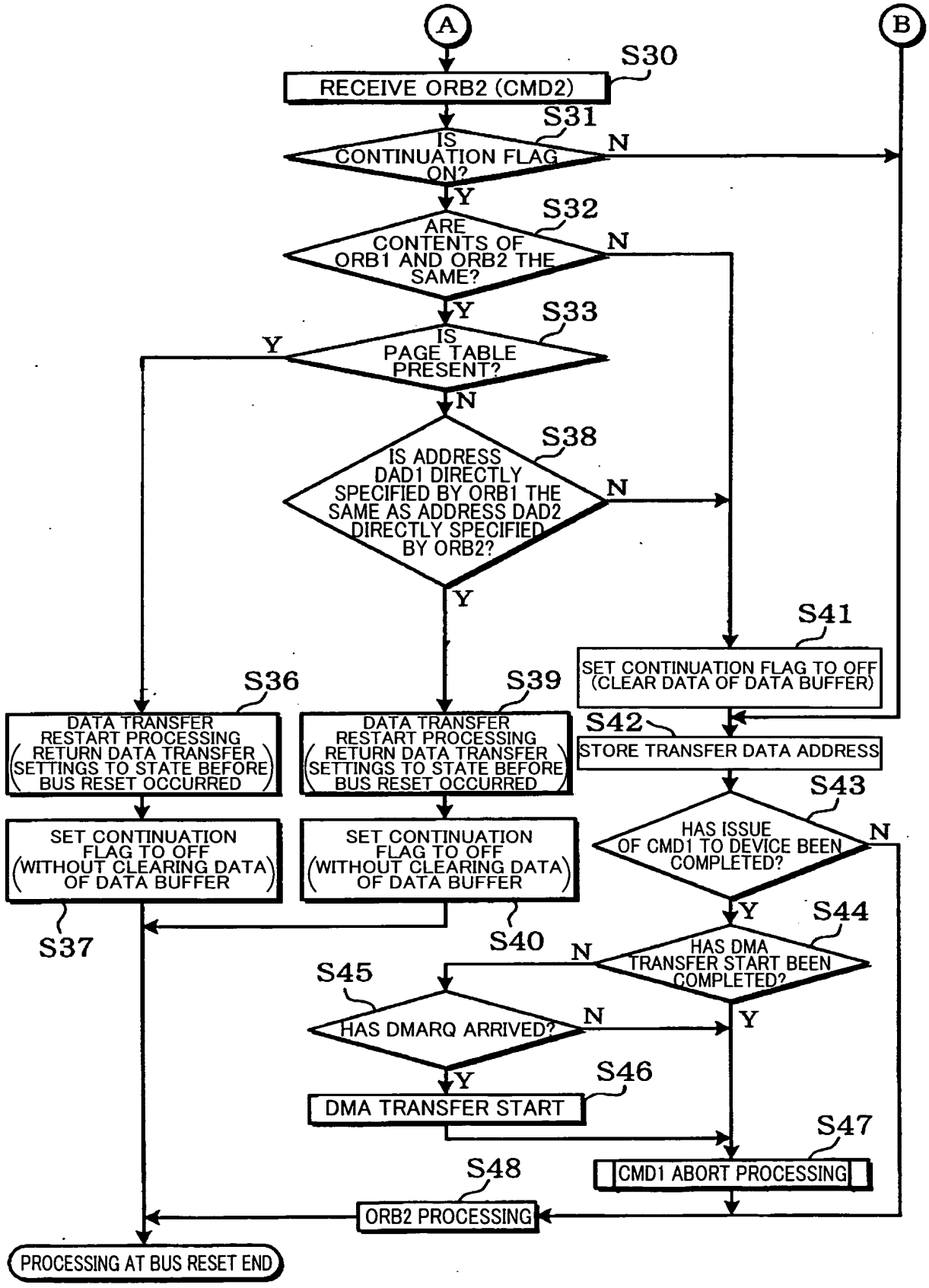


FIG. 25


A
B
S30
RECEIVE ORB2 (CMD2)
S31
IS CONTINUATION FLAG ON?
N
Y
S32
ARE CONTENTS OF ORB1 AND ORB2 THE SAME?
N
Y
S33
IS PAGE TABLE PRESENT?
Y
N
S38
IS ADDRESS DAD1 DIRECTLY SPECIFIED BY ORB1 THE SAME AS ADDRESS DAD2 DIRECTLY SPECIFIED BY ORB2?
N
Y
S41
SET CONTINUATION FLAG TO OFF (CLEAR DATA OF DATA BUFFER)
S36
DATA TRANSFER RESTART PROCESSING (RETURN DATA TRANSFER SETTINGS TO STATE BEFORE BUS RESET OCCURRED)
S39
DATA TRANSFER RESTART PROCESSING (RETURN DATA TRANSFER SETTINGS TO STATE BEFORE BUS RESET OCCURRED)
S42
STORE TRANSFER DATA ADDRESS
S43
HAS ISSUE OF CMD1 TO DEVICE BEEN COMPLETED?
N
Y
S44
HAS DMA TRANSFER START BEEN COMPLETED?
N
Y
S45
HAS DMARQ ARRIVED?
N
Y
S46
DMA TRANSFER START
S47
CMD1 ABORT PROCESSING
SET CONTINUATION FLAG TO OFF (WITHOUT CLEARING DATA OF DATA BUFFER
SET CONTINUATION FLAG TO OFF (WITHOUT CLEARING DATA OF DATA BUFFER
S37
S40
S48
ORB2 PROCESSING
PROCESSING AT BUS RESET END